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Scaling organic transistors: materials and design

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Envisaged applications of organic thin-film transistors in future polymer electronics lead to requirements on the supply voltage, threshold voltage, subthreshold characteristics, on-off ratio, and cut-off frequency. We present an analysis of the corresponding requirements using both analytical estimates and numerical two-dimensional simulations. Of special importance are the connections between cut-off frequency, channel length and mobility, mobility and doping, thicknesses of the active layer and gate insulator, doping, interface charges and states, and threshold voltage, traps and subthreshold slope. They lead to demands on both material properties and transistor design. Considering a minimum application-relevant cut-off frequency and a limitation of the mobility for low-cost solution-based deposition, one is led inevitably to the need of a submicrometer channel length and rather thin organic gate insulator. Experimental realization is shown and an approach to submicrometer organic CMOS is discussed.

Key words: *polymer electronics; transistor; organics; scaling*

1. Introduction

Novel polymer (or "plastic") electronics is expected to present its first commercial products within the next few years. Possible applications, such as electronic watermarks, E-paper, replacements of the barcode, and smart cards, are generally characterized as low-performance and low-cost in a region where silicon technology will not be competitive. As an additional special feature, the new circuits should be flexible. One vision is a large scale printing of such circuits. It was only about twenty years ago that scaling down became a decisive issue in microelectronics, when the feature length, especially the channel length of MOS transistors, was reduced below one micrometer. That development was connected to Moore's law describing the transition to higher packaging and increased speed [1]. For the development of polymer electronics based on organic field-effect transistors (OFETs), in spite of encouraging demonstrations of different applica-

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tions [2–4], there is actually a barrier for overcoming the minimum requirements for successful mass applications: scaling down of present OFETs is a *precondition*, even for the introduction of polymer electronics. In this article, the scaling of OFETs is outlined, based on analytical estimates and numerical simulations [5].

2. Analytical estimates

To begin with, some basic requirements should be mentioned. OFETs should operate at voltages less than 10 V. Correspondingly, a threshold voltage of only few volts and of the same polarity as the gate voltage (negative for a p-channel device) is needed (otherwise additional circuitry is required), connected with a subthreshold swing less than several hundred mV/dec. Thereby an on-off ratio of the current larger than 10^4 must be realized. The cut-off frequency (at which the voltage gain is reduced to unity) should be larger than 100 kHz.

The design and material parameters of OFETs are closely related. Most suitable polymers are thus unintentionally p-doped, source and drain are made from metals, and it is believed that inversion is hardly achievable. Therefore, thin-film transistors are used, which operate with an accumulation channel in the on-state. As a consequence, the off-state with depletion, and also clear saturation with depletion at drain, require a layer thickness d less than the depletion length l_{dep}, which in turn depends on the doping level ($l_{\mathrm{dep}} = [2\varepsilon\varepsilon_0|2\varphi_b|/eN_A]^{1/2}$, where $\varphi_b < 0$ is the bulk potential for the p-material, and N_A is the density of ionized acceptors). For poly(phenylene-vinylene) (PPV) and poly(3-alkyl thiophene) (P3AT), one has $l_{\mathrm{dep}} \approx 240$ nm up to 24 nm for doping levels from 10^{16} down to 10^{18} cm^{-3}. For high doping levels it becomes important to prepare layers in the 50 nm range and with small roughness compared to thickness.

The next important quantity is the threshold voltage, which is given for $d < l_{\mathrm{dep}}$ by

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + \frac{eN_A d}{C''_{ox}} - 2\varphi_b \left(\frac{d}{l_{\mathrm{dep}}} \right)^2 \tag{1}$$

where V_{FB} is the flat band voltage and $C''_{ox} = \varepsilon_0 \varepsilon_{ox}/d_{ox}$ is the gate insulator capacitance per a unit area. Only the first term is negative when a low-work function gate is chosen. The second term, in particular, contributes high positive values in the unwanted direction for high doping. The main dependences are demonstrated in Fig. 1 (parameters: 2 eV gap of the active layer, ε = 3.24, affinity 3 eV, gate work function 5 eV, ε_{ox} = 2.56 for the organic insulator, V_{FB} = 1 V + φ_{b}). According to Fig. 1a, the threshold voltage is sufficiently low for the considered layer thicknesses only at low and moderate doping (<10^{16}–10^{17} cm^{-3}). For higher doping (Fig. 1b), a strong increase in the threshold voltage can be prevented only by choosing both a thin insulator and a thin active layer. Indeed, for all-polymer circuits the most stringent requirement concerns the rather thin organic gate insulator. In addition, a shift in threshold voltage

can result from a flat band voltage shift caused by charges at the interface (areal charge $Q_{if}^{"}$) between the active layer and gate insulator, according to

$$V_{FB} = \Delta\Phi_{MS} - \frac{Q_{if}''}{C_{ox}''} = \Delta\Phi_{MS} - \frac{eN_{if}''d_{ox}}{\varepsilon_0\varepsilon_{ox}} \tag{2}$$

where $\Delta\Phi_{MS}$ is the gate-semiconductor work function difference. Such interface charges can occur unintentionally. For $N_{if}'' = 10^{12}$ cm^{-2} and ε_{ox} = 3, the flat band voltage is shifted by 3 V (18 V) for a gate insulator thickness of 50 nm (300 nm), again showing the importance of a thin organic insulator. In principle, by introducing such a charged layer, one can shift the threshold voltage in the needed direction.

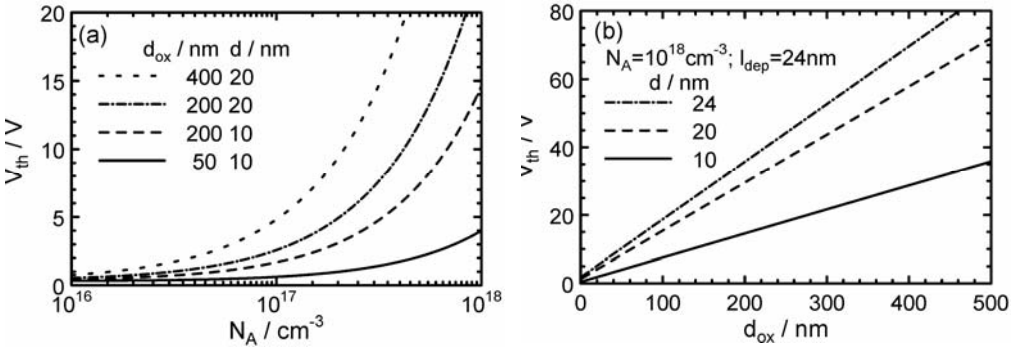

Fig. 1. Dependence of the threshold voltage in Eq. (1) on doping (a) and on gate insulator thickness (b) for the indicated parameters

For low-voltage transistor operation, the inverse subthreshold slope $S = \partial V_{GS}/\partial\lg(I_D)$, [A] must be as low as possible. At room temperature, its minimum value is 60 mV/dec, whereas experimental values for OFETs are often several V/dec, which is rather large. Actually, recharging the capacitances of the depletion layer and interface traps leads to higher values, according to

$$S = \frac{k_B T}{e}\ln 10\left(1 + \frac{C_{\text{dep}} + C_{it}}{C_{ox}}\right) \tag{3}$$

Bulk traps contribute to the depletion capacitance. For the trap-free case in a thin layer, the layer is depleted and one would have the ideal minimum value. Bulk and interface traps in the thin layer thus cause a deviation from the ideal minimum value. Corresponding numerical simulations will be shown below.

Most important for scaling OFETs is the cut-off frequency $f_0 = g_m/(2\pi C_{GS})$, which is determined by the maximum transconductance g_m and the gate-source capacitance C_{GS}, which is larger than the gate insulator capacitance due to overlap capacitances.

An upper limit for the cut-off frequency is obtained from the simplest approximation for the drain current of a transistor with channel length L and width w

$$f_0 \le \frac{1}{2\pi}\frac{g_m}{C''_{ox}wL} = \frac{\mu}{2\pi L^2}V_{GS,\mathrm{eff}} \tag{4}$$

where $V_{GS,\mathrm{eff}}$ is the gate voltage relative to threshold, for drain voltage $V_{DS} = V_{GS,\mathrm{eff}}$ pinch-off occurs and the transconductance has its maximum. The channel width cancels out in Eq. (4). For a given low operation voltage (e.g., $V_{GS,\mathrm{eff}}$ = 10 V) and sufficiently large f_0 (100 kHz, 1MHz, 10MHz) one gets from Eq. (4) the required upper limit for the channel length as a function of the mobility of the active layer, as demonstrated in Fig. 2. Thus, for the mobility μ = 0.01 $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$ (which seems to be achievable in low-cost solution deposition) and the lowest cut-off frequency, the upper limit for the channel length is already as small as 3 μm. Practically, one must expect that only submicrometer channel lengths will lead to the needed operation speed. Now another problem occurs: one must take care to avoid short-channel effects for such devices. These can be analyzed only by two-dimensional simulations.

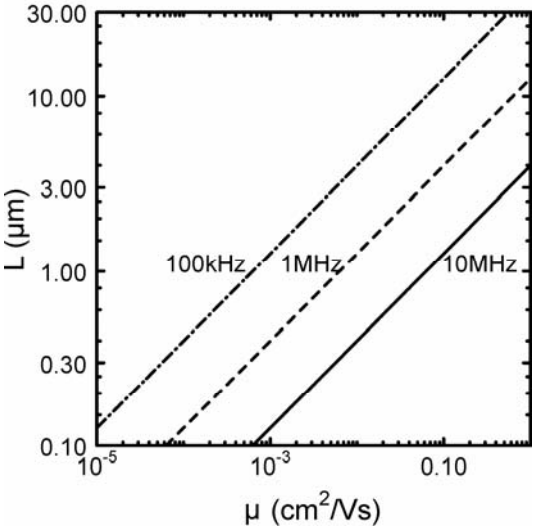

Fig. 2. Channel length as function of mobility, according to Eq. (4), which for a given effective voltage of 10 V leads to three different cut-off frequencies, namely 100 kHz, 1 MHz and 10 kMHz

3. Simulation of short-channel effects

As already discussed, down-scaling also concerns the gate insulator thickness, in order to enable operation at low voltage with an appropriate threshold voltage and reduced influence of possible interface charges. In addition, a thin gate insulator is needed to avoid short-channel effects. Since in a field-effect transistor the perpendicular field creating the accumulation channel must be much larger than the longitudinal field driving the current in the channel, the gate oxide thickness must be much smaller than

the channel length. From experience in microelectronics, one expects roughly the condition $d_{ox} < L/10$. Detailed information, however, requires two-dimensional simulations. They have been carried out by us in advance, before preparing short channel transistors. The method and standard parameters are described in the appropriate references [6, 7]. In the simulations the prepared device is modelled (see the cross section in Fig. 5).

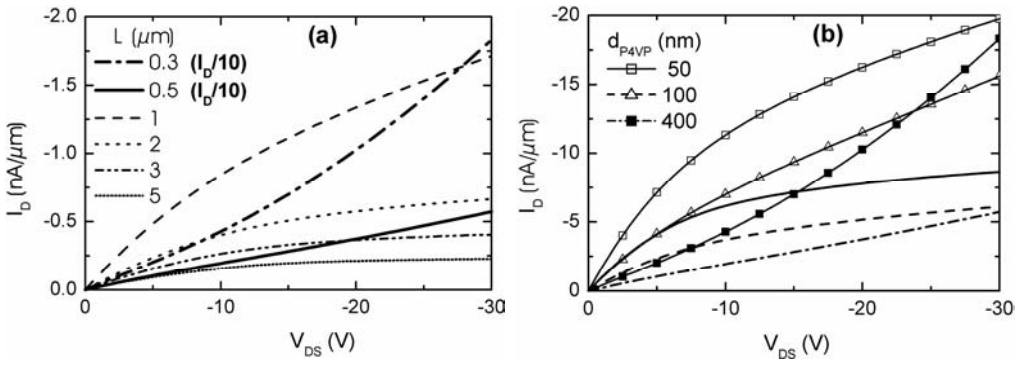

Fig. 3. Simulated output characteristics (current per unit channel width) for a 10 V gate-source voltage: a) for a 400 nm thick P4VP gate insulator the channel length is varied as indicated; b) for the two channel lengths 0,5 μm (lines) and 0,3 μm (with symbols), gate insulator thickness is varied. Other parameters: *p*-doping 10^{17} cm^{-3} of the 30 nm P3OT layer, mobility $\mu = 10^{-3}$ cm^2/(V·s)

In Figure 3a, the thickness of the organic insulator (poly-4-vinylphenol, P4VP) is 400 nm, as large as is practically realizable, in order to prevent leakage current. The output characteristics show saturation only for a channel length larger than 1 μm and a large supralinear current for shorter channels. Simulated field and concentration profiles prove that this is a short channel effect, due to drain-induced barrier lowering indeed caused by the decreasing ratio of transversal and longitudinal electric fields. A reduction of insulator thickness down to 50 nm for devices with 0.5 μm and 0.3 μm channel lengths reduces this effect, as shown in Fig. 3b. Such organic insulators are not yet available. Therefore, short-channel OFETs should be fabricated at present with a hybrid structure, in which the gate insulator is a thin (e.g. 30 nm) silicon dioxide layer on a n^+-silicon wafer that serves as the gate electrode. An example is given below.

4. Trap recharging and inverse subthreshold slope

In contrast to the ideal low value of the inverse subthreshold slope (Eq. (3)) and its need for the low voltage operation of organic transistors, one is usually confronted with rather large values [6, 8, 9]. An example is demonstrated in Fig. 4 [6] for a transistor with organics in the insulator and active layer. The source/drain contacts are deposited as finger structures on an organic substrate (poly(ethyleneterephthalate)), PET; channel length and width are L = 2 μm and w = 10 mm, respectively. Then the

active layer, the organic insulator, and gate are deposited. The active layer (30 nm) is made from regioregular poly(3-dodecylthiophene) (P3DDT), and the gate insulator (500 nm) from poly(4-vinylphenol) (P4VP). For this device, the peculiarities in the subthreshold region have been described in detail in [6, 10], and a few main results will be summarized here. The transistor turns on (Fig. 4a) close to a threshold voltage of V_{th} = 0 V, indicating that the layer is fully depleted at positive gate voltages. Consequently, the maximum possible value of the doping concentration is $N_A \approx 6\times10^{17}$ cm^{-3}. The mobility estimated from the linear region of the transfer characteristics of Fig. 4a is $\mu_p = 5\times10^{-3}$ cm^2/(V·s) for drain voltages of –5 V and –10 V, and $\mu_p = 2\times10^{-3}$ cm^2/(V·s) for –1 V. The inverse subthreshold slope, estimated from the transfer curves in the logarithmic scale, is very large. For V_{DS} = –1 V one has S = 7.7 V/dec. Moreover, the subthreshold current depends on the drain voltage. This feature is usually considered to be a short channel effect, not expected for the investigated long channel device. To clarify the origin of such peculiarities, numerical two-dimensional simulations have been carried out. Thereby the mobilities, as determined from experimental data, have been used, along with the following parameters: static dielectric constants of both materials, ε_{ox} = 2.56 for P4VP and ε = 3.24 for P3DDT, a monomer density of 10^{21} cm^{-3}, and a work function of the gate, drain, and source electrodes (Au) of 5.0 eV.

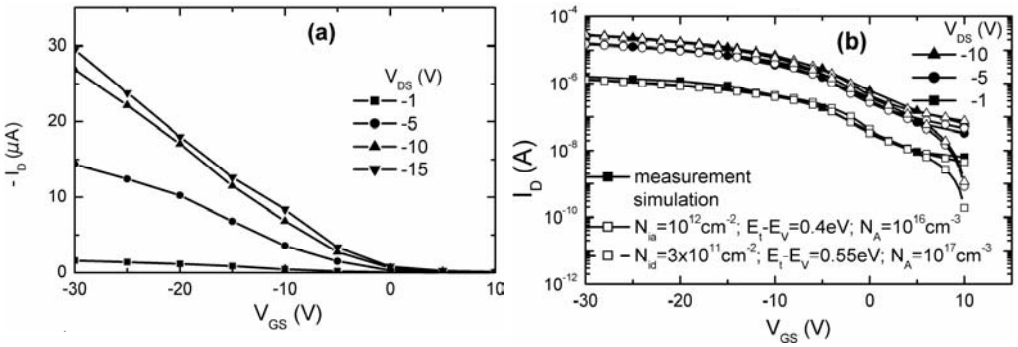

Fig. 4. Measured transfer characteristics of a thin film transistor with w/L = 5000, L = 2 μm (a); comparison of the measured and simulated transfer characteristics in a logarithmic scale for different drain voltages (b). Parameters for the acceptor-like or donor-like interface states are indicated in the figure

In the first step, the doping concentration was varied. According to Eqs. (1) and (2), the threshold voltage and hence all transfer characteristics are determined not only by doping, but also by fixed interface states. Above the threshold voltage the curves measured are well described by simulations with either $N_A = 10^{16}$ cm^{-3} without fixed interface states or with a higher doping concentration and positive interface charge. However, there is a large difference in the subthreshold region between the measured and simulated characteristics. Whereas the measured curve has the mentioned large inverse subthreshold slope, the simulation yields $S \approx 0.2$ V/dec. Furthermore, in con-

trast to the measurement, the simulated transfer characteristics approach a common subthreshold dependence. According to Eq. (3), the inverse subthreshold slope can be influenced either by interface or bulk traps. A systematic variation of acceptor concentration N_A, the concentration N_{ia} and energy of acceptor-like interface states (neutral if empty and negative if occupied by an electron), or the concentration N_{id} and energy of donor-like interface states, has shown that there is no influence of trapped interface charges on the drain current above the threshold voltage. In the off-state, however, the inverse subthreshold slope depends strongly on the occupancy of interface traps. Recharging with varying gate voltage then leads to the observed degradation of the inverse subthreshold slope and also to the drain voltage dependence of the subthreshold current. The experimental dependencies can actually be well described with either acceptor-like traps and lower acceptor doping (Fig. 4b) or with donor-like interface states and higher acceptor doping. The corresponding concentrations and positions of the trap energy level relative to the valence band are indicated in the Figure. In both cases, there is good agreement of the curves above the threshold voltage and in the subthreshold regime up to a gate voltage of 5 V. At higher voltages, the simulated curves with acceptor-like interface traps better describe the experimental data. The simulations thus reveal that anomalous subthreshold characteristics, with an extremely large inverse subthreshold slope and a drain voltage dependence of the subthreshold current, can arise from a recharging of interface states. Apart from interface traps, variations in bulk charges, caused for example by bulk traps, can also lead to such peculiarities [10]. To achieve the required low inverse subthreshold slope, materials and preparations are needed that avoid deep bulk and interface traps.

5. Submicron transistors by underetching

As described above, one must expect that only devices with submicrometer channel lengths lead to the needed OFET operation speed. Different patterning techniques, such as screen printing [11], soft lithographic stamping [12], and inkjet printing [13], have demonstrated neither the desired resolution nor alignment accuracy as yet. Photolithography [2] is expected to be too costly for the submicrometer regime. Recently, Stutzmann et al. [14] used embossing to fabricate vertical-channel field-effect transistors with submicrometer channel lengths, but could not observe saturation in the measured output characteristics.

We have developed [15, 5] high performace submicrometer channel length polymer field-effect transistors using only standard low-cost microelectronic techniques. In order to prevent short-channel effects, one needs also a rather thin gate insulator. Since until now no organics are available for this purpose, we used a hybrid technology – a 30 nm silicon dioxide layer on a highly doped silicon wafer serving as a gate. Source and drain, separated from each other by a short channel (1 μm or less in length), are fabricated by gold sputtering, low resolution photolithography, underetching, and the lift-off technique [15]. Finally, the active layer is spin coated. We used

soluble poly(3-octylthiophene) (P3OT) and poly(3-hexylthiophene) (P3HT), which are unintentionally highly doped. To enable the off-state of the transistor, the layer thickness must be less than the depletion length. In our case, the thickness is as low as 30 nm, which is controlled by the spin coating process. Until now no scanning electron microscope (SEM) images of the cross sections of prepared OFETs have been published. Indeed, due to a low atomic weight of the polymer constituents, imaging requires special techniques. A perpendicular cut through a prepared OFET with 1 μm channel length was been prepared [16] using the focused ion beam (FIB) technique. Previous electrical measurements have proven a good performance of the device (see below). In order to visualize the surface of the top layer made of P3HT, an additional layer of gold was been evaporated (40 nm). The resulting SEM image* (5 kV, sample tilted by 45°) is shown in Fig. 5. As a guide for the eye, the structure is repeated schematically in the lower part. Notice the thin gate insulator, the short channel between source and drain, and the additional top gold layer to mark the P3HT surface.

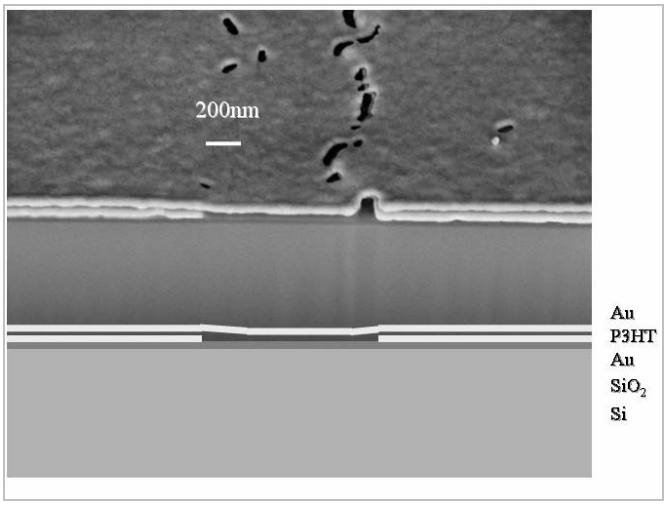

Fig. 5. SEM image of the cross section of an OFET with 1 μm channel length. The lower panel shows a schematic view

As an example of electrical properties, the output and transfer characteristics are depicted in Fig. 6. They demonstrate the following advantages: (i) operation at voltages lower than 5V, (ii) pronounced saturation of the output characteristics, (iii) only marginal short channel effects, (iv) a high on-off ratio (10^4), (v) a small inverse subthreshold slope (S = 0.5 V/dec), and (vi) negligible contact resistances. Hysteresis effects are still characteristic of OFETs [7, 17, 18]. In our case they are negligible for the drain voltage sweep at a given gate voltage (Fig. 6a), but different characteristics are obtained by decreasing or increasing the gate voltage. This is seen clearly in the

* The FIB–SEM image has been taken by Dr. S. Menzel [16].

transfer characteristics (Fig. 6b and c). The associated shift of the threshold voltage, however, is less than 1 V and thus small compared to literature values. Since the used P3AT were not specially treated, mobility is still low ($(2–3)\times10^{-5}$ $cm^2/(V\cdot s)$).

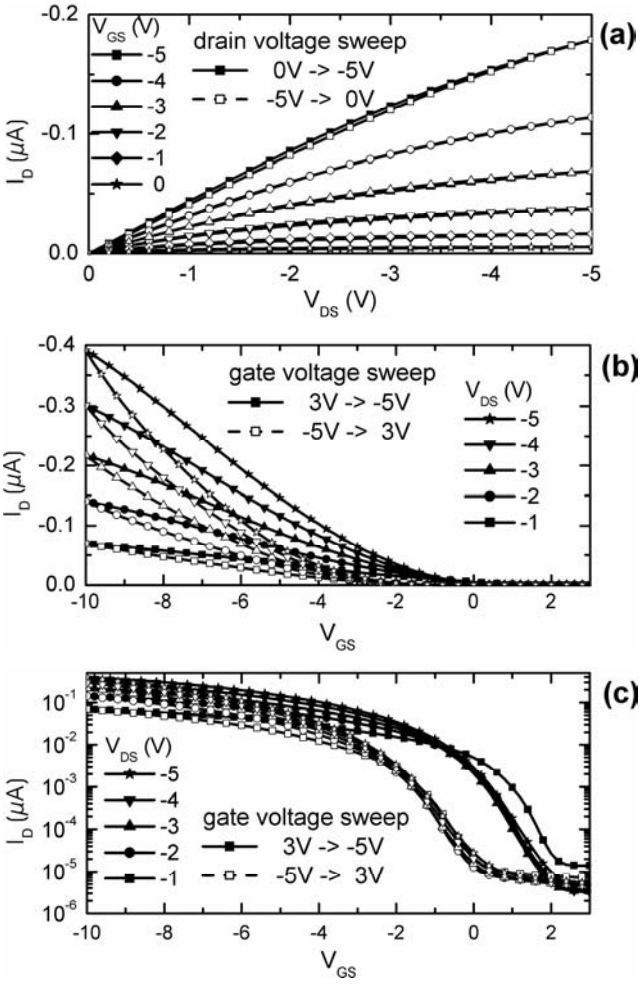

Fig. 6. Output characteristics of a P3HT transistor with a channel length of L = 740 nm and channel width of w = 1000 μm at different gate voltages and sweep directions (the hold and delay times are 180 s and 1 s, respectively) (a) ; transfer characteristics of the same transistor for different drain voltages and sweep directions: linear scale (b) and logarithmic scale (c); (the hold and delay times are 180 s and 10 s, respectively)

The success is that submicrometer OFETs with such a good performance can be fabricated without high-resolution lithography, and using only well established low-cost microelectronics processes. Before reaching the above mentioned goals, however, several problems remain unsolved. First, the mobility of the active layer must be enhanced by modifying the material and deposition process. Also, a thin organic gate

insulator material is needed. Finally, circuits must be fabricated on plastic substrates, and in order to achieve high frequencies, parasitic capacitances must be reduced. The latter requires a self-aligned gate. Finally, for effective CMOS (complementary metal oxide semiconductor), circuits, n-channel devices are also needed.

6. Towards submicrometer organic CMOS

Until now, few n-channel OFETs have been described in literature [19, 20]. However, they are not likely for a common preparation with p-channel OFETs as submicron devices on the same substrate in a low-cost. In connection with recently prepared ambipolar OFETs, it has been suggested that they can serve as both p-channel and n-channel devices in CMOS circuits [21, 22]. In order to minimize power consumption in such circuits, one of the transistors (e.g. the n-channel OFET) should be in the off-state and the other in the on-state. Ambipolar OFETs, however, do not have an off-state with a sufficiently low current. Moreover, the current levels of both devices should be of the same order of magnitude.

Several rules can be formulated that lead to a proposal for n-channel OFETs for CMOS circuits. These rules are based on published results of single-layer (interpenetrating) networks of poly-[2-methoxy-5-(3′,7′-dimethyloctyloxy)]-p-phenylene vinylene (OC1C10-PPV) and [6,6]-phenyl C61-butyric acid methyl ester (PCBM), precursor-pentacene [21]) and hetero-layer ambipolar OFETs (pentacene as the hole transport layer and N,N′-ditridecylperylene-3,4,9,10-tetracarboxylic diimide (P13) as the electron transport layer [23]), on our simulations of a single-layer model ambipolar OFET [24], on simulations of top contact and bottom contact OFETs [25], especially with a Schottky-type material for source and drain, and on improved carrier injection by contact modification in organic light emitting diodes (OLEDs) [26]. The main problem with n-channel OFETs lies in the low affinity of the appropriate active layer organics, which is around 3 eV. This makes it hard to find a material for source/drain with a work function that is also comparably low. Even Mg (the work function from 3.6 eV to 3.7 eV) has an extremely large electron barrier, effectively a Schottky-type contact to the electron accumulation channel. According to our simulations [25], in this case the current for a top contact may be larger by orders of magnitude than that for a bottom contact. Nevertheless, the barrier is so large that one can hardly achieve balanced electron and hole currents, since good accumulation contacts are possible for the holes (e.g. with Au). The effect of this large barrier for electrons can be reduced in a way similar to OLED [26] (in this case, for the hole injecting anode) by an intermediate thin layer with somewhat larger affinity (between 3 eV and 3.6–3.7 eV) leading to a staggered barrier. Even then electron injection is still worse than hole injection at the Au accumulation contact. An active material is needed in which not only electron and hole mobilities are both large (c.a. $\mu = 0.01$ $cm^2 \cdot V^{-1} \cdot s^{-1}$), but one in which electron mobility is the larger of the two. Results on a hetero-layer ambipolar OFET indicate that pentacene is a suitable candidate. Although the P13

layer was intended as an electron conducting layer, according to our simulations [24], both the p-channel and n-channel are formed in the pentacene layer and the P13 layer leads to a staggered barrier at the Mg top contact. For low-cost and solution-based preparation, the formation of pentacene from a soluble precursor [27] is preferred.

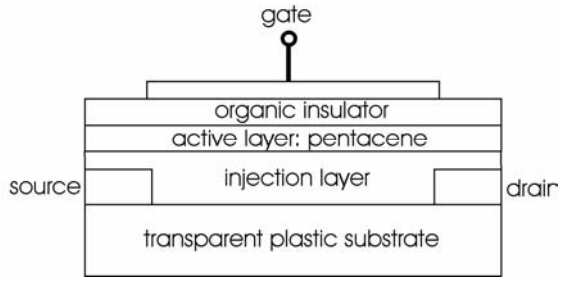

Fig. 7. Design of n-channel OFETs

A design for an n-channel OFET according to these considerations is shown in Fig. 7. The layer with an affinity larger than that of the active layer is denoted as the injection layer. Since the low-cost underetching technique for the preparation of submicron channel lengths [15] has already been realized with gold on a plastic substrate (Mylar), it should also work with Mg if an appropriate etching agent is used. For the design of the p-channel with Au as source and drain, no injection layer is needed. Problems to be solved include the need for a sufficiently thin and solution-processible organic gate insulator and the preparation of a self-aligned gate. For the latter, a recently published method [28] should be adapted. With an optically transparent substrate, source and drain can serve as an opaque optical mask for the gate definition.

7. Conclusions

A breakthrough in polymer electronics requires thin film-transistors that operate at voltages below 10 V. A threshold voltage of only a few volts and of the same polarity as the gate voltage is needed, connected with a subthreshold swing less than several 100 mV/dec. Thereby an on-off ratio of the current larger than 10^4 must be realized. The cut-off frequency should be larger than 100 kHz. Considering the connections between material properties and design, corresponding demands for the devices can be formulated. Since in low-cost solution-based fabrication the electron and hole mobilities can hardly exceed values of 10^{-2} cm^2/Vs, scaling down the channel length to the submicrometer region seems inevitable. For the definition of such short channels, an effective and cheap method based on underetching has been developed recently [15]. In addition, an (organic) gate insulator thickness less than 50–100 nm is required in order to avoid short channel effects. Analysis of transport and injection leads to a proposal for the design of n-channel OFETs suitable for CMOS circuits.

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