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PTFE encapsulation for pentacene based organic thin film transistors*

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Unprotected organic devices suffer from degradation due to water and oxygen incorporation. To validate the function of organic thin film transistor capsulation, interdigital transistor structures (W/L = 16 830 and W/L = 23 400) were prepared on p-type silicon wafers, and a high current was driven (initially up to –15 mA and –6.8 mA, respectively, at $-40V_{DS}$, $-40V_{GS}$) in order to detect their explicit reactions to degradation. Subsequently, the OTFT active layer was encapsulated with 1.5 μm of sputtered polytetrafluoroethylene (PTFE). The degradation experiment for 4 months in dark laboratory conditions revealed reduced degradation compared to earlier experiments using thinner protection films. During the experiment, the threshold voltage shifted in the positive direction, suggesting degradation only due to oxygen. Obviously, degradation due to humidity was blocked, as it would have caused a negative threshold voltage shift.

Key words: *pentacene; OTFT; interdigital structure; degradation; encapsulation*

1. Introduction

Organic semiconductor materials such as small-molecule pentacene provide many advantages when used in electronic devices. They are cheap, easily processed at relatively low temperatures [1, 2], and allow the use of flexible substrates [3, 4]. In contrast, the degradation of organic semiconductor materials is still an unsolved problem. The electrical properties of organic thin film transistors (OTFT) suffer from contact with oxygen, humidity, and UV light. Calculations have revealed a high probability of oxygen-forming a stable chemical bond with the middle ring of pentacene in a reaction leading to pentacenequinone [5]. Embedded in a crystalline pentacene film, this

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molecule serves as a scattering (trapping) centre for charge carriers in the OTFT channel [6] and would affect the electrical performance of the device, i.e. reduce the on-current, decrease the on-off ratio, and shift the threshold voltage in positive direction [7]. Humidity is incorporated in the organic film from ambient air while the transistor is operating. Driven by the electrical field induced by the operating voltages at the drain and gate, water molecules dissociate and attach to the grain boundaries of the pentacene layer and to the dielectric interface [6]. At the grain boundaries, trapping states and disturbing potential walls are generated, resulting in a decrease of charge carrier mobility.

Accumulated at the dielectric interface of the OTFT, water molecules cause a threshold voltage shift in the negative direction. A degradation experiment with unprotected OTFTs kept in dark laboratory conditions for a period of 9 months (ambient air, room temperature) revealed a decrease in the on-current of one order of magnitude per quarter of a year [8]. Meanwhile, the threshold voltage shifted from the value of 4.8 V to –8 V. After the investigation period, the OTFT still showed typical output and transfer characteristics, however the electrical parameters had been strongly affected. Even if OTFTs are intended for use in short term applications, the operational lifetime should reside in a period of several months in order to guarantee the secure functioning of the organic circuits. To extend transistor shelf life, an encapsulation of the organic film against environmental effects seems to be essential. Lee et al. [9] have proposed a lamination process with an Al film, which, however, still needs an additional insulation layer to prevent shortcuts between the drain- and source-contacts. The deposition of additional layers on the pentacene in the channel area of an OTFT must be carried out very prudently, as the morphological structure of the organic film can be impaired. This letter presents a sputtering procedure with polytetrafluoroethylene (PTFE) at a low deposition rate and sputtering energy for encapsulating the pentacene film.

Organic field-effect transistors were prepared using two layouts. Small transistors with $W = 1000$ µm and $L = 1$ µm were fabricated to investigate the influence of oxygen plasma treatment on pentacene film formation during organic semiconductor evaporation. Interdigital structures with $W = 46.8$ cm and $L = 20$ µm, as well as $W = 16.83$ cm and $L = 10$ µm, were integrated for testing PTFE capsulation. These should drive a large current and a clear reaction should be detected due to external effects, and they should still provide a measurable current after months of degradation.

2. Experimental

Bottom contact OTFTs (Fig. 1) were fabricated on p-type silicon substrates instead of polymeric substrate materials for the degradation experiments, in order to exclude side effects from the unintended degradation of the substrate. The gate oxide layer was grown by thermal oxidation at 960 °C up to a thickness of 150 nm, determined by laser ellipsometry. Subsequently, the drain and source contacts were defined using UV contact photolithography and lift-off in acetone. The drain and source contacts consisted of a thin (8 nm) nickel layer and nearly 80 nm of gold, while the sub

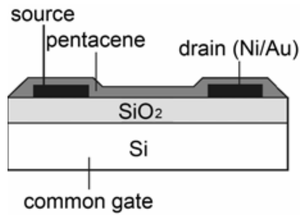

Fig. 1. Cross-section of an OTFT based on a silicon substrate using the organic semiconductor pentacene

strate served as the common gate contact. Previously to the thermal evaporation of up to 30 nm of pentacene at 6×10^{-7} mbar, the wafers were treated in oxygen plasma for 30 s at low power (100 W). This was done to prepare the dielectric surface for pentacene deposition and to remove residual resist at the contact edges. By this treatment, the diameter of the pentacene crystallites was increased from 250 nm (on untreated silicon oxide) to nearly 1 µm (on the treated wafer) as confirmed by AFM (Fig. 2).

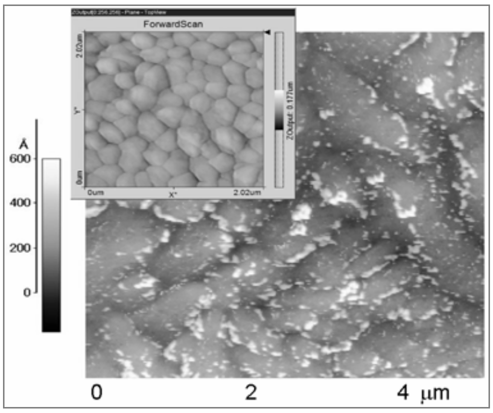

Fig. 2. Large grains of pentacene on SiO_2 treated with oxygen plasma (AFM image, contact mode). Inset: small grains of pentacene evaporated on an untreated dielectric. Both images have the same scale

Finally, after the first electrical characterization an interdigitally structured OTFT (W/L = 23 400) was encapsulated with a sputtered layer of 1.5 µm PTFE. The deposition rate was as low as 21 nm/min and the circular gradient was below 10%. A detailed description of the experimental conditions and deposition technique are given elsewhere [10]. All electrical characterizations were carried out in a shielded metal box in dark laboratory conditions with a HP 4156A semiconductor parameter analyzer.

3. Results and discussion

One of the main advantages of photolithographically defined OTFTs is the high geometrical reproducibility of fabricated structures. Compared to earlier experiments [7, 8], a uniform distribution of electrical parameters was now achieved, introducing a tight feedback of favourable preparation conditions to the fabrication process. The distribution of threshold voltages on a 100 mm wafer showed a strongly emphasized Gaussian peak at (1.3±1.44) V for a small OTFT geometry of $W = 1000$ µm and $L = 1$ µm (Fig. 3).

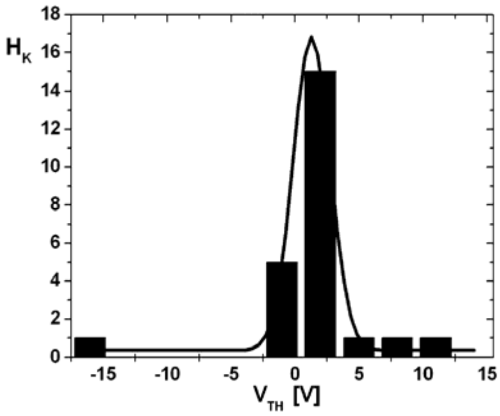

Fig. 3. Distribution of threshold voltages measured for photolithographically structured OTFTs ($W = 1000$ µm, $L = 1$ µm) on a 100 mm wafer. The pentacene was thermally evaporated on a SiO_2 dielectric without previous oxygen plasma treatment. The final thickness of pentacene was 30 nm

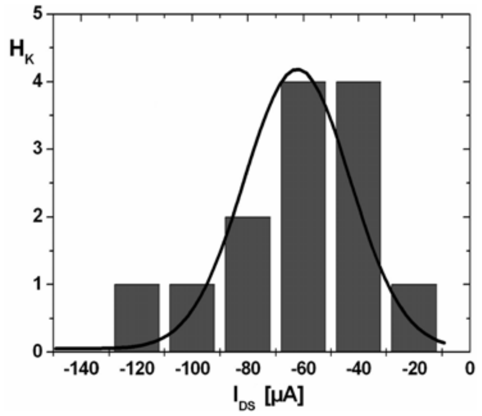

Fig. 4. Distribution of the on-currents measured at $-40V_{DS}$ and $-40V_{GS}$ for OTFTs with $W = 1000$ µm and $L = 1$ µm, providing a pentacene layer of 30 nm

The maximum on-current at $-40V_{DS}$ and $-40V_{GS}$ for these devices was measured to be as large as –(63.3±17) µA (Fig. 4). By introducing oxygen plasma treatment of the gate dielectric layer before pentacene deposition, the on-current of a comparable OTFT structure was enhanced up to –644 µA for $-80V_{DS}$ and $-25V_{GS}$. An inspection of the pentacene surface using an atomic force microscope confirmed large pentacene grains in the transistor channel, compared to smaller grains of the untreated pentacene film (Fig. 2). This results in a decreased number of grain boundaries and traps across the channel. Unfortunately, the increase in the on-current was accompanied by a large positive threshold voltage of 15.9 V. This is attributed to the plasma treatment, which leaves behind plenty of trapping states at the dielectric interface. In a preliminary encapsulation experiment, the above stated OTFT ($I_{DS} = -644$ µA) was coated with a thin PTFE layer 20 nm thick. As a result of the high power sputtering process, however, the transistor exhibited a strong decrease in electrical parameters, as the pentacene film was obviously affected by the PTFE deposition. OTFTs with a larger W/L ratio were then structured with the intention of supplying a measurable current in the following degradation experiment.

Interdigitally structured OTFT with the W/L ratio of 16 830 was prepared and characterized directly after pentacene deposition. The on-current was found to be as large as –15 mA for $-40V_{DS}$ and $-40V_{GS}$ (Fig. 5), due to the large W/L ratio. The threshold voltage was extracted from the square root current of the transfer characteristic (Fig. 6). This remained at a rather high value of 7 V due to the above mentioned trapping states induced by the plasma treatment and to a large channel area, which provides numerous free charge carriers inhibiting the depletion of the channel. As a result of the large threshold voltage, the calculated charge carrier field effect mobility was 2.6×10^{-2} $cm^2/(V\cdot s)$.

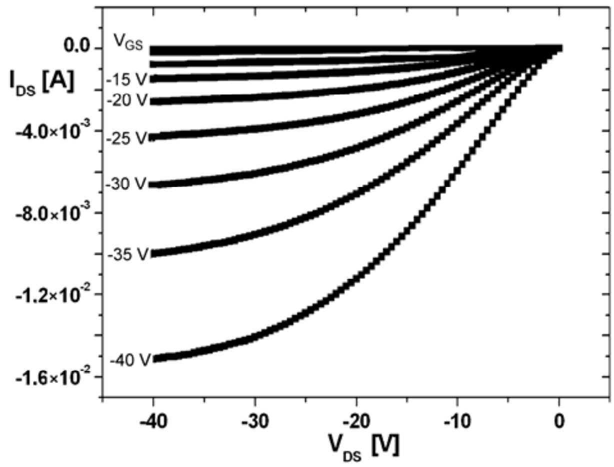

Fig. 5. I_{DS}–V_{DS} characteristics of an OTFT with W = 16.83 cm and L = 10 µm, providing a 30 nm pentacene layer, evaporated at 6×10^{-7} mbar on a substrate cleaned with oxygen plasma

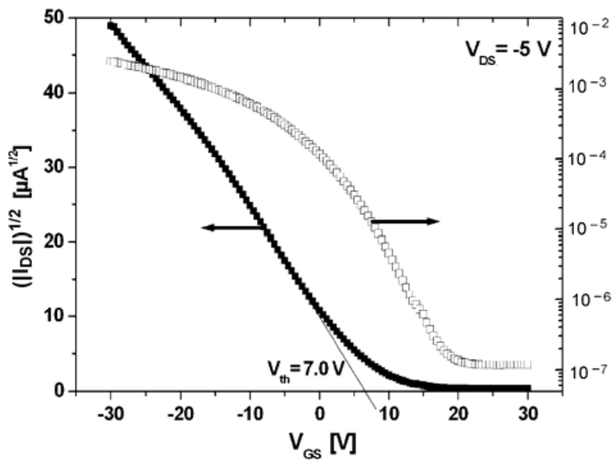

Fig. 6. I_{DS}–V_{GS} characteristics of the same OTFT as in Fig. 5. An on-off ratio of more than 10^4 and a threshold voltage of 7 V can be extracted from the transfer curve

Another interdigital OTFT structure (W/L = 23 400) was prepared for the degradation experiment. The transistor maximum on-current was determined to be as large as –6.8 mA and the threshold voltage was 12.3 V before the pentacene was covered with PTFE. After sputtering 1.5 µm of PTFE onto the surface of the interdigital OTFT structure at low power, the initial values of the electrical parameters for the degradation experiments were measured (I_{DS} = –6.2 mA, V_{TH} = 13.2 V). This characterization was repeated periodically after 1 month of degradation.

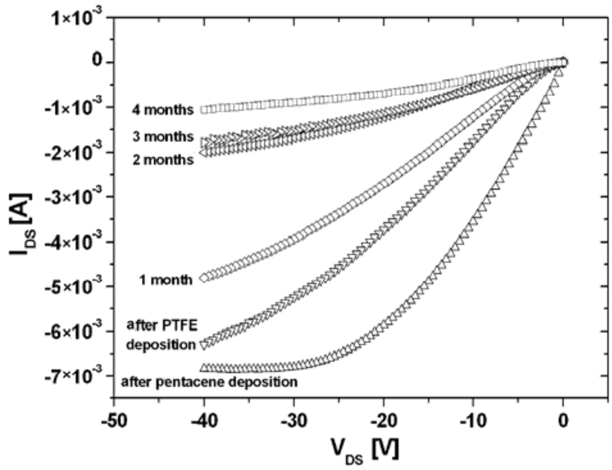

Fig. 7. I_{DS}–V_{DS} characteristics at $-40V_{GS}$ for an OTFT with W/L = 23 400 using a nearly 30 nm thick pentacene layer. The measurements were carried out directly after pentacene evaporation, PTFE deposition, and in intervals of 1 month for a period of 4 months, and represent the reduction of the on-current due to degradation. As a second reaction to the degradation experiment, the contact resistance was influenced, which can be deduced from the bending of the characteristics in the linear region

In Figure 7, one can see the time-dependent behaviour of the transistor on-current at $-40V_{GS}$. For the first 2 months of degradation the on-current was reduced significantly (–4.7 mA, –1.9 mA), but the rate of the degradation seemed to slow down at least after 3 months of investigation (–1.7 mA, –1.1 mA). Earlier experiments revealed a decrease in the OTFT on-current of one order of magnitude per quarter of a year for an unprotected pentacene layer stored in comparable conditions [8]. In the current experiment, a strong degradation of the transistor parameters was obviously inhibited by the PTFE layer. Nevertheless, the threshold voltage shifted from an initial value of 13.2 V directly after sputtering to 18.2 V (after 1 month) and 23.2 V (after 4 months). This threshold voltage shift cannot be neglected but one has to keep in mind that the initial value was rather high. As the PTFE layer is hydrophobic in character, it protects the pentacene from reacting with humidity. Oxygen can still diffuse through the encapsulation and cause threshold voltage shift. As reported elsewhere, oxygen induces a positive threshold voltage shift in organic field effect transistors [7]. The effect of humidity on the degradation of transistor parameters, however, is much larger and would evoke a negative shift in the threshold voltage as reported before [8].

Even if the required shelf life of organic circuits in single-use applications is rather limited, the secure functioning of OTFTs must be guaranteed. PTFE films may be recommended as capsulation layers on pentacene transistors to prevent degradation by humidity and to enhance the shelf life of transistors.

4. Conclusions

This paper reports a reproducible fabrication of organic field effect transistors, using photolithography to structure the devices and thermally evaporated pentacene films as the organic semiconductor. Oxygen plasma was applied to clean the dielectric surface before the deposition of pentacene and to ensure large organic crystallites in the transistor channel. With this treatment, the maximum on-current of the transistor was notably enhanced. Interdigital OTFT structures with a W/L ratio of 23 400 were prepared for the degradation experiments. The pentacene layer was encapsulated with 1.5 µm of PTFE and stored for 4 months in laboratory conditions. The on-current at $-40V_{DS}$ and $-40V_{GS}$ was reduced from an initial value of –6.2 mA to –1.1 mA after 4 months of degradation. Compared to unprotected samples, the rate of degradation was strongly reduced. A positive threshold voltage shift occurred, indicating that humidity can be excluded as a degradation factor. Oxygen may have diffused through the PTFE layer. Earlier experiments revealed a positive threshold voltage shift due to the presence of oxygen.

Acknowledgements

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