Materials Science-Poland, Vol. 25, No. 4, 2007

Nanocluster memories by ion beam synthesis of Si in SiO_2*

B. SCHMIDT[1**], K.-H. HEINIG[1], L. RÖNTZSCH[1], K.-H. STEGEMANN[2]

[1]Research Center Dresden Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden, Germany

[2]ZMD AG, Dresden, Germany[***]

Ion implantation and ion irradiation induced interface mixing were used to synthesise silicon nanoclusters in the gate oxide of metal–oxide–semiconductor (MOS) structures aiming at electronic memory applications. In the present study silicon nanocrystals for multi-dot floating-gate memories produced by ion irradiation through SiO_2/Si nterfaces have been investigated to demonstrate possible advantages of this approach compared to conventional application of ion beam synthesis to the fabrication of silicon nanocrystal memories. The memory properties of the fabricated structures as a function of Si^+-irradiation dose and post-irradiation annealing temperature and time have been examined through electrical measurements on n-channel MOS field-effect transistors. Low-voltage operating devices that can endure more than 10^6 programming/erasing cycles have been successfully achieved. More research is still required to improve charge retention and ensure the standard 10-year retention time needed for true non-volatile memory applications.

Key words: ion beam synthesis; silicon nanocrystal; nonvolatile memories

1. Introduction

At conventional low- and medium-fluence ($<10^{16}$ ions/cm^2) ion implantation in microelectronics the concentration of introduced dopants is usually below their solubility limit in silicon. At certain annealing temperatures, the impurity atoms are dissolved in Si and located on crystal lattice sites or, as a small part, remain as soluted interstitial atoms.

At high-fluence ($\geq 10^{16}$ ions/cm^2) ion implantation, or at so-called ion beam synthesis (IBS), a far-from-equilibrium state (supersaturated solid) is achieved which relaxes towards thermodynamic equilibrium during subsequent annealing by phase

---

*Presented at the 2ndWorkshop "Hybrid Nanostructured Materials. Synthesis, Properties, Applications", Dresden, Germany, 8–9 November, 2006.

**Corresponding author, e-mail: Bernd.Schmidt@fzd.de

***Now at Signet Solar GmbH Dresden, Germany

separation through precipitation and ripening (Ostwald ripening) of nanoclusters (NC) [1] (Fig. 1). Phase separation of ion implanted, immiscible impurity atoms from the surrounding matrix, i.e. the formation of NCs, can also occur during the implantation process if the impurity atoms are sufficiently mobile due to collisional ion mixing; otherwise a subsequent annealing is always necessary.

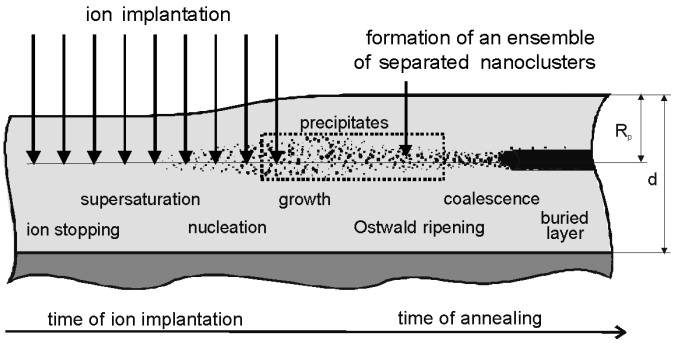

Fig. 1. Scheme of ion beam synthesis of nanostructures. High dose ion implantation into a solid leads to supersaturation of impurity atoms. NCs nucleate and grow during ion implantation or, for impurity atoms immobile during implantation, during subsequent thermal treatment. The mean NC size as well as their spatial and size distributions changes during the Ostwald ripening. At very high fluences, buried layers can form by coalescence of NCs

Although there are possibilities to tailor the mean NC size (mainly by variation of ion fluence and annealing temperature and time) at conventional IBS the possibilities for tailoring the NC size distribution by the variation of ion implantation parameters are rather limited.

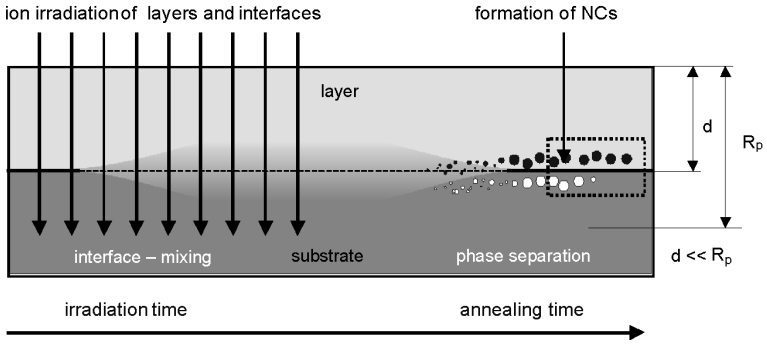

Fig. 2. Scheme of ion beam induced self-alignment of a NC δ layer near the layer/substrate interface by ion irradiation through the interface and subsequent thermal treatment leading to the phase separation in the ion mixed non-stoichiometric near-interface layer through precipitation and Ostwald ripening of NCs

Ion irradiation not only causes supersaturation and damage to the substrate but also affects the interface between the thin layer and the substrate or interfaces between

thin stacked layers. As schematically shown in Fig. 2, primary energetic ions produce collisional cascades which cause substantial interface mixing leading to non-stoichiometric and non-stable phases near the interface. Subsequent annealing restores the interface region rapidly via spinodal decomposition. However, the tails of the mixing profiles do not reach the recovered interfaces by diffusion, thus, phase separation proceeds via nucleation and growth of NCs near the interface. The competition between interface restoration and nucleation self-aligns nearly monodispersive δ layers of NCs in proximity to the interface. Recently, self-organization of a δ layer of Ge NCs in SiO_2 has been found [2, 3] close to the Si/SiO_2 interface after appropriate Ge^+ implantation into a SiO_2 layer on a Si substrate. The NC δ layers were found when the following conditions were fulfilled : a negligibly small amount of ions is implanted in the Si/SiO_2 interface region (i), and the cascade of energetic O and Si recoils produced by primary collisions produces a few displacements per atom (dpa) in the Si $/SiO_2$ region (ii). Different contributions to the self-organization and self-alignment of NC δ layers have been described and investigated and predicted by kinetic MC simulations and reaction-diffusion equations [4]. Very recently, this prediction has been verified experimentally by transmission electron microscopy [5, 6].

The IBS of semiconducting NCs has attracted much interest due to their compatibility with CMOS technology and due to unique physical properties of NCs as zero-dimensional objects. A great effort is currently devoted to their applications in new microelectronic devices, e.g. charge storing Si and Ge NCs in non-volatile memory circuits [7–10]. An example is the non-volatile multi-nanocrystal floating-gate memory proposed by Tiwari et al. [11]. The idea of this novel NC memory concept is simple: in comparison to conventional MOSFETs the only evolutionary step is the replacement of the poly-Si floating gate by a layer of electrically isolated Si NCs. However, the fabrication of monodispersive and small Si NCs (≤ 3 nm) separated from the transistor channel by a thin (2–3 nm) oxide represents a strong challenge. At the common IBS of Si NCs, low energy ion implantation into SiO_2 with ion energies lower than 5 keV and relatively high ion fluences in the order of $(1–2)\times10^{16}$ cm^{-2} is applied [8, 9]. Alternatively, the approach for ion irradiation induced self-alignment of Si NCs near SiO_2/Si interfaces can also be applied to the fabrication of non-volatile multi-dot floating gate memory devices [12]. The present contribution will be addressed to self-organization processes of silicon nanoparticles during ion irradiation of flat Si/SiO_2 interfaces during Si^+ ion irradiation and to the fabrication of Si NC memory devices using this approach.

2. Experimental

A MOS-like $Si/SiO_2/Si$ structure was selected and submitted to Si^+ ion irradiation to mix the interfaces of this layer stack. The ion irradiation experiments were carried out on 6” (100)Si wafers covered with a 15 nm thermally grown SiO_2 layer and a 50 nm

poly-Si layer deposited by LPCVD on top of the SiO_2 layer. The upper poly-Si layer was used as a capping layer to prevent any influence of contaminants from ambient and annealing atmosphere (mainly humidity) on the NC formation process in the gate oxide [13]. The poly-Si/SiO_2/Si stack was irradiated with 50 keV Si^+ ions at fluences in the range of 3×10^{15}–1×10^{16} cm^{-2}. After ion irradiation a highly n^+-doped and 250 nm thick poly-Si gate was deposited onto the irradiated stack. Subsequently, the samples were annealed (RTA) at various temperatures (950–1100 °C) and times (5–180 s) and further processed for the fabrication of nMOSFETs in the standard 0.6 μm CMOS process line of the ZMD company [14]. Transistors with long-channel (20 μm) and short-channel (0.6 μm) gate length and 20 μm gate width have been fabricated and tested.

3. Results

During ion irradiation, through a MOS-like Si/SiO_2/Si structure unstable non-stoichiometric SiO_x ($x < 2$) phases are formed, sandwiched between stable phases of SiO_2 and Si. Annealing restores the upper and lower SiO_2/Si interfaces by spinodal decomposition. However, the tails of the Si atom mixing profiles do not reach the recovered interfaces by diffusion thus, the phase separation proceeds via nucleation and growth of Si NCs in SiO_2. The competition between interface restoration and nucleation self-aligns δ layers of Si NCs in SiO_2 along the two interfaces. This self-alignment of δ layers of Si NCs with the SiO_2/Si interfaces has been predicted by atomistic computer simulations [15]. As shown in Fig. 3, Si precipitates in SiO_2 have developed to Si NC δ layers which are aligned with the SiO_2/Si interfaces. The mean Si NC diameter is 2 nm and the mean distance from the interfaces is 2 nm, too. In each δ layer, the Si NC areal density is in the order of 10^{12} cm^{-2}. This prediction has been verified experimentally by energy filtered transmission electron microscopy (EFTEM) [6]. As can be seen in Fig. 4, bright and dark areas are visible in dark and white regions of the SiO_2 layer, respectively. These spherical regions refer to Si NCs in the oxide. Accordingly, the Si NCs are separated from the SiO_2/Si interfaces by a mean distance of 3 nm, i.e. they are aligned in a δ layer at each interface. The mean diameter of the NCs was estimated to be 3 nm. These morphological features are in accordance with the KLMC simulation from [15].

Electrical measurements of memory properties show that devices exhibit significant memory windows at low gate voltages. Devices with a memory window of about 0.5 V for write/erase voltages of ±7 V and the programming time t_{pp} of 10 μs have been achieved. In terms of memory window and transistor characteristics, an implanted fluence of $(5–7)\times10^{15}$ Si^+ cm^{-2} and annealing at T_A =1050 °C for t_A = 30 s appear as promising conditions for device fabrication (Fig. 5a). The memory window can be increased by annealing at higher temperatures (1100 °C) and/or for longer time (over 120 s) resulting in a further phase separation and Si NC formation. As shown in Fig. 5b, in this case a large stable memory window of ΔV_{th} ~ 3 V can be achieved.

No degradation in memory windows was observed for devices after 10^7 write/erase cycles with V_{pp} = +7V/–7V, t_{pp} = 1 ms programming conditions (Fig. 6), which means that the fabricated memory devices exhibit a superior endurance (very limited degradation up to 10^7 cycles). It was found that data retention time tested at 85 °C is

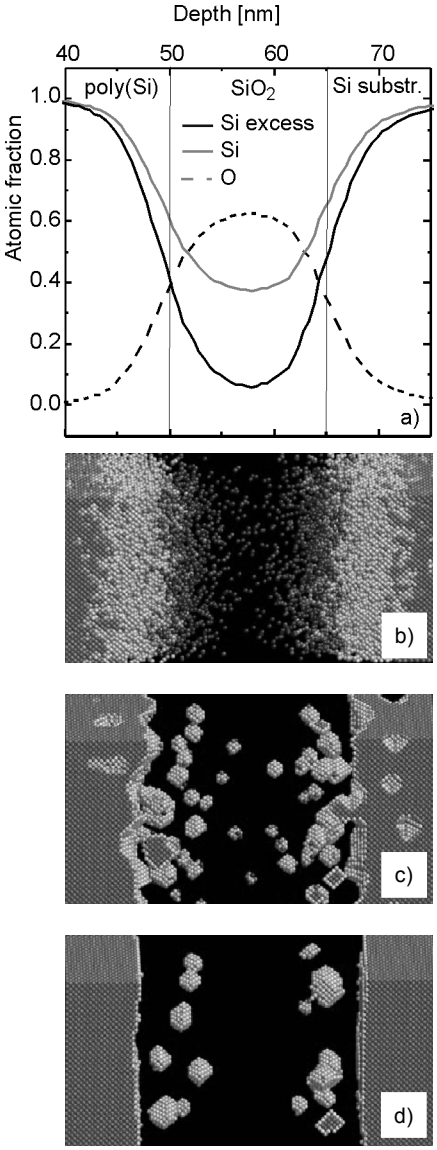

Fig. 3. Self-aligned Si NC formation by ion irradiation of SiO_2/Si interfaces: a) TRIDYN results of Si ion irradiation (E = 50 keV, $D = 1\times10^{16}$ cm^{-2}) through a layer stack of 50 nm poly-Si, 15 nm SiO_2, into the Si substrate. KLMC simulation snapshots referring to: b) the as-irradiated state, c) the early state of phase separation, d) to a later stage

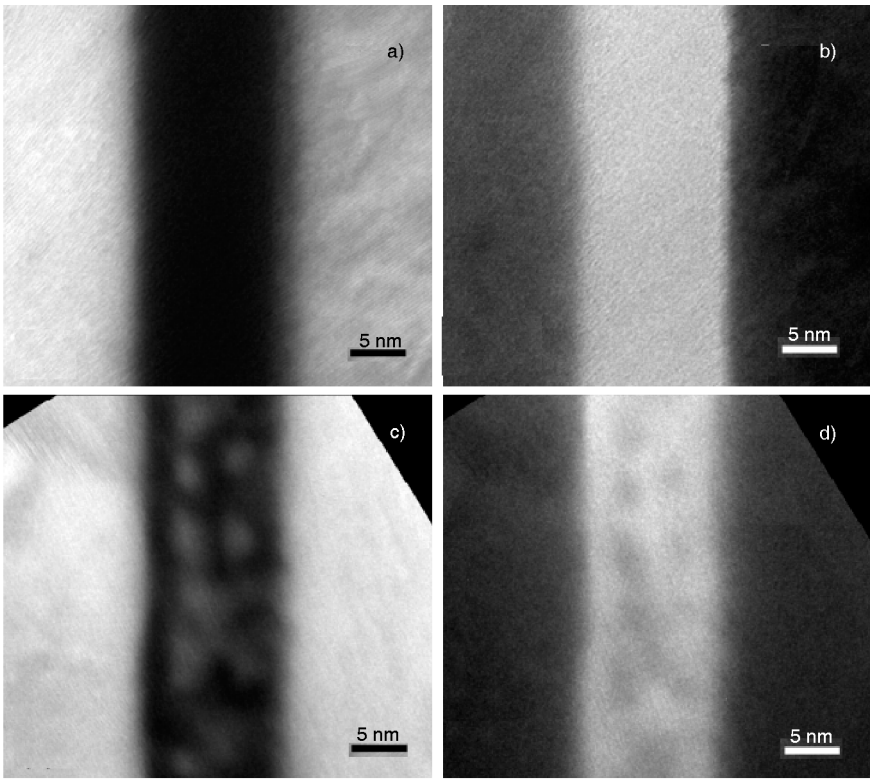

Fig. 4. Energy-filtered XTEM images of the poly-Si/SiO_2/Si structure: a, b) referring to the as-deposited state, c, d) after Si^+ ion irradiation (E = 50 keV, $D = 7\times10^{15}$ cm^{-2}) and post-irradiation annealing (T = 1050 °C, t = 120 s)

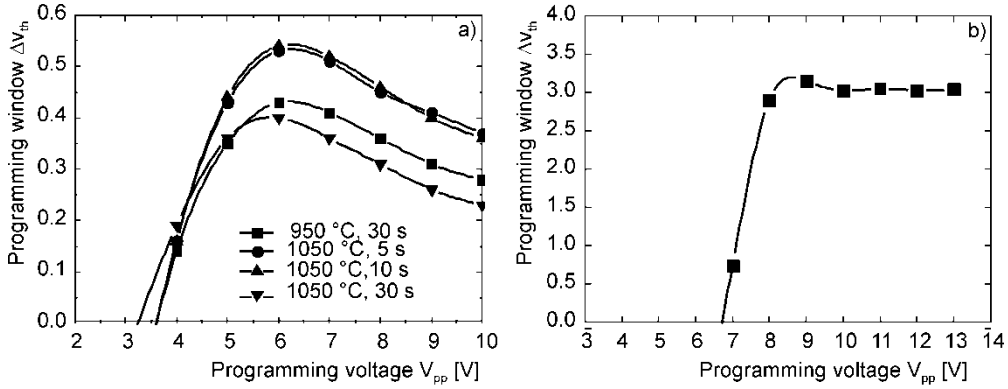

Fig. 5. Memory window ΔV_{th} vs. programming voltage V_{pp} (pulse length t_{pp} = 10 ms) of n-channel MOSFETs with self-aligned Si NCs in the gate oxide. Si^+ irradiation was performed at the ion energy of 50 keV and the fluence of 7×10^{15} cm^{-2}: a) for low thermal budget at various RTA annealing parameters, b) for high thermal budget and annealing at 1050 °C for 120 s

too low for EEPROM application (100 days at room temperature and 8 h at 85 °C). The fabricated nMOS devices exhibit maximum memory windows at low gate voltages indicating that the charge storage nodes are located near to the Si/SiO_2 interface. This implies the possibility of direct charge carrier tunneling into Si NCs during low programming voltages. The lowering of the programming window at programming voltages $V_{pp} > 6$ V (Fig. 5a) can be explained by trap-assisted tunneling through the gate insulator.

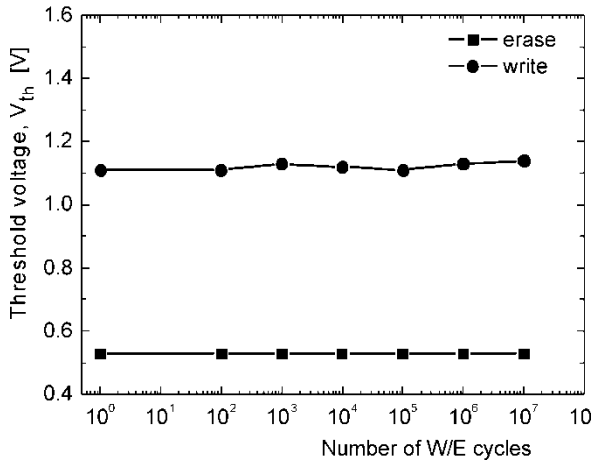

Fig. 6. Endurance characteristics of *n*MOSFETs obtained with write/erase voltages V_{pp} of ±7 V and pulses t_{pp} = 1 ms. The sample was irradiated with 50 keV Si^+ ions at the fluence of 7×10^{15} cm^{-2} and annealed at 1050 °C for 30 s

Besides retention, all electric parameters of the devices fulfil current requirements for non-volatile memory devices. The low data retention might be explained by direct re-tunneling of charge carriers to the channel which could be a common problem of multi-dot floating-gate memories.

4. Discussion

From structural examination of Si^+ ion irradiation induced self-organization of Si NCs in SiO_2, carried out using energy filtered transmission electron microscopy (EF-TEM) we conclude that the diameter of the NCs is smaller than 3 nm. Independent experiments using special techniques for decoration of the tiny Si precipitates by Ge or Si also demonstrated their existence [4, 5]. Additionally, for samples annealed after ion irradiation, ToF-SIMS [16] verifies two δ layers of Si excess within SiO_2. One δ layer is close to the upper Si/SiO_2 interface, the other is close to the lower one. Each δ

layer is separated from its interface by a narrow zone of ~ 3 nm denuded of Si excess, which is in agreement with our MC simulations.

The fabricated nMOS devices exhibit large memory windows at very low gate voltages, e.g. 1.9 V for 10 ms ±6 V and 3 V for 10 ms ±9 V) similar to the ones measured also on MOS capacitors indicating that the charge storage nodes are located near the Si/SiO_2 interface. This implies the possibility of direct charge carrier tunneling into Si NCs during low programming voltages. The lowering of the programming window at programming voltages $V_{pp} > 6$ V (Fig. 5a) can be explained by partial charge loss of the lower NC δ layer towards the gate and/or charging of the upper NC δ layer.

Besides retention, all electric parameters of our device fulfil current requirements. The low data retention might be explained by direct re-tunneling of charge carriers to the channel which could be a common problem to improve charge retention and ensure the standard 10-year retention time needed for true non-volatile memory applications. A fast charge loss could be avoided by an asymmetric tunneling behavior, e.g. by tunneling oxide engineering [17]. To solve this problem, additional studies are necessary.

Table 1. Ion beam synthesis of Si NCs in SiO_2; low energy Si^+ ion implantation into SiO_2 in comparison with ion irradiation through Si/SiO_2 interfaces

Si^+ ion implantation into SiO_2	Si^+ ion irradiation through interfaces
Unprotected gate oxide: serious impact of the ambient during processing	Gate oxide protected by poly-Si: no contamination by impurities and/or humidity during processing
Low energy, high dose implantation: strong sputtering and swelling of SiO_2	Irradiation with low fluences: no sputtering and no swelling of SiO_2
NC location due to implantation: difficulty to place NCs close to channel (ion energy critical)	NCs due to ion beam mixing: self-alignment of NC layer close to the channel (ion energy is not critical)
Ions and recoils come to rest in the interface region: degradation of the channel	Ions come to rest deep within Si: defects do not deteriorate the channel

Compared to conventional IBS of Si NC in SiO_2 by direct Si^+ ion implantation into thin SiO_2 layers ion irradiation through Si/SiO_2 interfaces results in some processing advantages which are summarized in Table 1. The protection of thin gate oxide by a poly-Si during processing (ion beam and thermal treatment) suppresses contamination by impurities and/or humidity [13] which can influence significantly the NC formation process. Compared to low energy and high dose ion implantation

into SiO_2 [10, 18, 19], the irradiation with relatively low fluences does not cause sputtering and/or swelling of the thin SiO_2 layer which is an important result from the technological point of view. Due to ion beam mixing, where the ion energy is not a critical parameter, a thin layer of nearly mono-dispersive Si NCs self-aligns close to the transistor channel. Furthermore, the ion energy can be selected in such a way that the ions come to rest deep within the Si substrate and remaining defects after annealing (end-of-range defects) do not deteriorate the transistor channel. Therefore, at ion beam synthesis of Si NCs in the transistor gate oxide, the ion beam mixing delivers a more stable process compared to direct ion implantation into thin SiO_2 layers.

5. Conclusion

Ion irradiation assisted formation of Si NC is appropriate for discrete charge trapping memories where no direct Si implantation into SiO_2 is required. No particular processing issues have been encountered during integration of this technique in standard sub-micron CMOS technology. The predictions of theoretical studies of ion irradiation assisted formation of Si NC δ layer are confirmed by experimental investigations. 0.6 μm n-channel MOSFETs with Si NCs in a 14.5 nm gate oxide were fabricated which exhibit charging at very low voltages and programming times in the ms range. The high endurance of 10^7 at low current consumption and short retention time are determined by the charging/decharging of the Si NCs by (direct) tunneling due to the location of the NCs close to the MOSFET channel.

Acknowledgement

This work was a part of the NEON project supported by the EC as GROWTH GRD1-2000-25619. The authors especially thank M. Perego and T. Gemming for carrying out ToF-SIMS measurements and EF-TEM investigations, respectively. The authors also would like to thank P. Dimitrakis and E. Votintseva for characterization of nMOSFETs by electrical measurements.

References

[1] REISS S., HEINIG K.H., Nucl. Instr. Meth. Phys. Res. B, 102 (1995), 256.
[2] HEINIG K.H., SCHMIDT, MARKWITZ A., GRÖTZSCHEL R., STROBEL M., OSWALD S., Nucl. Instr. Meth. Phys. Res. B, 148 (1999), 969.
[3] VON BORANY J., GRÖTZSCHEL G., HEINIG K.H., MARKWITZ A., SCHMIDT B., SKORUPA W., Sol.-State Electron., 43 (1999), 1159.
[4] HEINIG K.H., MÜLLER T., SCHMIDT B., STROBEL M, MÖLLER W., Appl. Phys. A, 77 (2003), 17.
[5] RÖNTZSCH L., HEINIG K.H., SCHMIDT B., MÜCKLICH A., Nucl. Instr. Meth. B, 242 (2006), 149.
[6] RÖNTZSCH L., HEINIG K.H., SCHMIDT B., MÜCKLICH A., MÖLLER W., THOMAS J., GEMMING T., Phys. Stat. Sol. (a), 202 (2006), R170.
[7] BEYER V., VON BORANY J., [in:] *Materials for Information Technologies*, E. Zschech, H. Mikolajick, (Eds.), Springer, Berlin, 2005, 139.

[8] NORMAND P., KAPETANAKIS E., DIMITRAKIS P., TSOUKALAS D., BELTSIOS K., CHERKASHIN N., BONAFOS C., BENASSAYAG G., COFFIN H., CLAVERIE A., SONCINI V., AGARWAL A., AMEEN M., Appl. Phys. Lett., 83 (2003), 168.
[9] NORMAND P., KAPETANAKIS E., DIMITRAKIS P., SKARLATOS D., BELTSIOS K., TSOUKALAS D., BONAFOS C., BENASSAYAG G., CHERKASHIN N., CLAVERIE A, VAN DEN BERG J.A., SONCINI V., AGARWAL A., AMEEN M., PEREGO M., FRANCIULLI M., Nucl. Instr. Meth. Phys. Res. B, 216 (2004), 228.
[10] MÜLLER T., HEINIG K.H., MÖLLER W., BONAFOS C., COFFIN H., CHERKASHIN N., BENASSAYAG G., SCHAMM S., ZANCHI G., CLAVERIE A., TENCÉ M, COLLIEX C., Appl. Phys. Lett., 85, (2004), 2373.
[11] TIWARI S., RANA F., HANAFI H., HARSTEIN A., CRABBE E., Appl. Phys. Lett., 68 (1996), 1377.
[12] SCHMIDT B., HEINIG K.H., RÖNTZSCH L., MÜLLER T., STEGEMANN K.H., VOTINTSEVA E., Nucl. Instr. Meth. Phys. Res. B, 242 (2006), 146.
[13] SCHMIDT B., GRAMBOLE D., HERRMANN F., Nucl. Instr. Meth. B, 191 (2002), 482.
[14] http://www.zmd.de
[15] RÖNTZSCH L., HEINIG K.H., SCHMIDT B., Mater. Sci. Semicond. Proc., 7 (2004), 357.
[16] PEREGO M., private communication.
[17] CASPERSON J.D., BELL L.D., ATWATER H.A., J. Appl. Phys., 92 (2002), 261.
[18] BONAFOS C., CARRADA M., CHERKASHIN N., COFFIN H., CHASSAING D., BENASSAYAG G., CLAVERIE A., J. Appl. Phys., 95 (2004), 5696.
[19] CARRADA M., CHERKASHIN N., BONAFOS C., BENASSAYA,G G., CHASSAING D., NORMAND P., TSOUKALAS D., SONCINI V., CLAVERIE A., Mater. Sci. Eng. B, 101 (2003), 204.

Received 2 July 2007