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Properties and estimated parameters of a submicrometer HSDMAGFET

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Main features and predicted values of key parameters of a novel magnetic field sensitive semiconductor device, horizontally-split-drain magnetic field sensitive field effect transistor (HSDMAGFET) which can be used to measure or detect steady or variable magnetic fields have been presented. Operating principle of the transistor is based on one of the galvanomagnetic phenomena and the gradual channel detachment effect (GCDE). The predicted relative sensitivity of the sensor can reach as high value as 100 [%/T]. Furthermore, due to its original structure, the spatial resolution of the MAGFET is extremely high, which makes this device particularly useful in reading magnetically encoded data or magnetic pattern recognition. Besides, a novel device related to the HSDMAGFET, namely, horizontally-split-drain current controlled field effect transistor (HSDCCFET) has been presented.

Key words: *magnetic field effect transistor (MAGFET); magnetic field measurement; magnetic pattern recognition*

1. Introduction

Density of magnetically recorded information on disk storage devices, magnetic field patterns, transaction cards, etc. has increased over the years, therefore development of magnetic field sensors and systems reading magnetically encoded data requires a continued improvement in magnetic field sensitive field effect transistor (MAGFET) performance [1–3]. Spatial and magnetic resolutions of MAGFETs are parameters of crucial importance [1, 2].

To meet requirements for key parameters of a magnetotransistor, a novel structure, horizontally-split-drain magnetic field sensitive field effect transistor (HSDMAGFET) has

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been proposed. It is pointed out that the expected high performance of the sensor could be improved when the vertical dimensions of the drain separation structure would be in the nanometer range. The structure, operating principle of the novel magnetotransistor, and its spatial resolution have been described. Magnetic sensitivity of the transistor has been predicted, and a novel device related to the HSDMAGFET, namely, horizontally-split-drain current controlled field effect transistor (HSDCCFET) has been presented.

2. MAGFET structure and its spatial resolution

The basic structure of the horizontally-split-drain magnetic field sensitive field effect transistor with n-type channel [4] is shown in Fig. 1. The device is a two-drain and two-gate enhancement-mode MOS type transistor in which the drain regions are placed one under the other and isolated from each other with a horizontal insulator

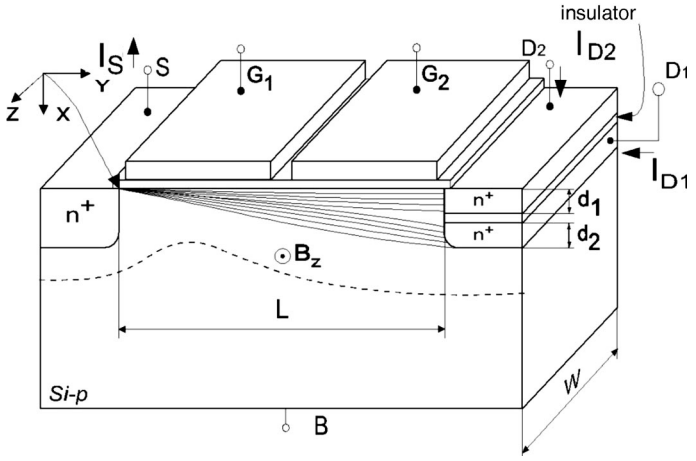

Fig. 1. Basic structure of the novel transistor [4]

layer. Positive voltages of the gates G_1 and G_2, V_{GS1} and V_{GS2}, induce an n-type channel in the transistor, and positive drain voltages, V_{DS1} and V_{DS2}, cause electrons to flow from the source S to the drains D_1 and D_2. The source current splitting electron streams flowing in the drains D_1 and D_2 is a consequence of a two-dimensional nature of kinetic processes in the transistor. Two-dimensional carrier flow is especially revealed when the magnitude of the drain-source voltages is higher than that of V_{GS}. Under this condition, the direction (the sense) of the transverse component of the electric field acting on the semiconductor surface in the vicinity of the drain is opposite to that of the source, which leads to repelling the negatively charged electrons from the semiconductor surface. Thus trajectories of mobile channel carriers are deflected downwards. This phenomenon can be called gradual channel detachment effect (GCDE). In turn, GCDE and non-uniformly distributed current of the carriers in the channel region

cause the channel of the transistor to spread out by diffusion – channel thickness modulation effect (CTME) takes place. Thus, these phenomena lead to gradually thicken and move away the electron stream from the semiconductor surface as values of the drain voltages are increasing. The effects stem from self-diffusion of mobile carriers and two-dimensional electric field distribution in the transistor channel (cf. e.g., [5, 6]). The GCDE and CTME are illustrated in Fig. 1 and clearly presented in Figs. 2 and 3 where the simulated electron concentration distributions in the transistor channel region are shown.

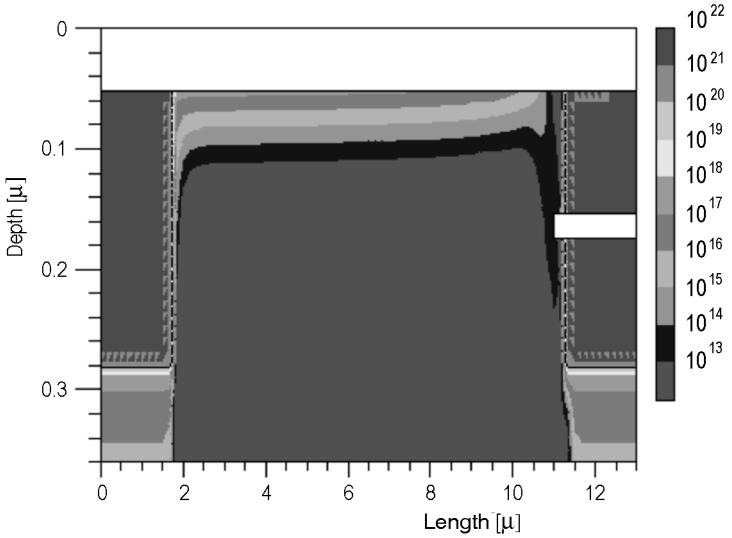

Fig. 2. Simulated electron concentration [cm^{-3}] distribution in an HSDMAGFET; $V_{DS1} = V_{DS2} = 9.2$ V, $V_{GS} = 1$ V, $B_z = 0$ T, $t_i = 20$ nm

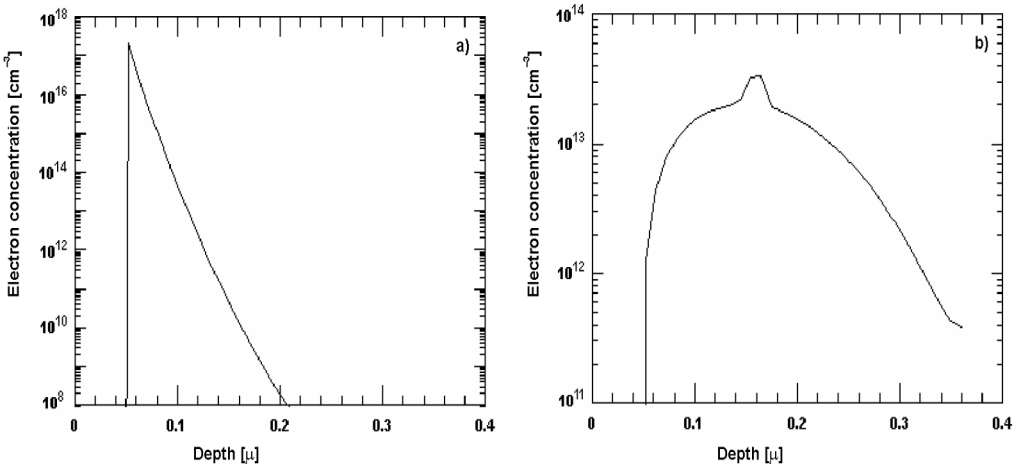

Fig. 3. Simulated electron concentration profiles for two cross sections made at abscissas $X_1 = 4000$ nm (a), and $X_2 = 11\,000$ nm (b) of the transistor channel of the HSDMAGFET shown in Fig. 2

A two-dimensional picture of the electron distribution in an HSDMAGFET with only one gate presented in Fig. 2 is obtained with the use of PISCES IIB program under the following biasing conditions: drain-to-source voltages $V_{DS1} = V_{DS2} = 9.2$ V, gate-to-source voltage $V_{GS} = 1$ V, the external magnetic induction z-component $B_z = 0$ T; thickness of the splitting insulator layer is equal to 20 nm. Figure 3 depicts more precisely simulated electron concentration profiles for two cross sections made at the abscissas $X_1 = 4$ μm and $X_2 = 11$ μm of the transistor channel of the HSDMAGFET shown in Fig. 2. For that specific bias of 9.2V at both drains, the drain currents I_{D1} and I_{D2} are equal to each other.

Referring to Figs. 1–3, we can assume the charge carriers in the channel to flow in the form of thin current layers while the Gauss law and the current continuity equation are fulfilled within each layer. Thicknesses of the drain regions, d_1 and d_2, and the splitting insulator layer t_i are assumed to be as small as possible and practically in the range of tens of nanometers.

The basic equation for the terminal currents of the device reads:

$$I_S = I_{D1} + I_{D2} \tag{1}$$

where I_S is the current injected into the channel through the source potential barrier, and I_{D1} and I_{D2} are currents flowing into the drains D_1 and D_2, respectively. Potential of the gate G_1 with respect to the source, V_{GS1}, determines the magnitude of I_S, and potential of the gate G_2, V_{GS2}, affects the ratio of current partition I_{D1}/I_{D2}. Thus the balance between drain currents can be achieved by changing the voltage V_{GS2}.

If we place the HSDMAFET in an external magnetic field, the Lorentz force acts on electrons moving in the channel [3]. Consequently, the magnetic induction z-component B_z (Fig. 1) causes the current layers in the channel region to deflect up or down, depending on the direction of B_z. This leads to an asymmetry in the terminal drain currents, which is a measure of the magnetic field strength. An imbalance between the drain currents, defined as $\Delta I = I_{D1} - I_{D2}$, is a function of the transistor channel width W, channel length L, biasing voltages V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, and magnetic induction $\boldsymbol{B}$, which can be expressed as [7]

$$\Delta I = I_{D1} - I_{D2} = f(W, L, V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, B_z) \tag{2}$$

As to the structure and principle of operation, the novel MAGFET is very similar to Popovic and Baltes's SDMAGFET, [3, 8] presented in Fig. 4. The SDMAGFET also comprises two drains, but they are placed side by side and vertically insulated, cf. Figs. 1 and 4. In Popovic's and Baltes's sensor, the x-component B_x of the magnetic field deflects current lines in the plane yz and finally an imbalance between I_{D1} and I_{D2} occurs, so the SDMAGFET is a sensor of the perpendicular-to-gate component of the magnetic field.

Magnetic field sensitivity and spatial resolution are basic parameters for an HSDMAGFET. The sensitivity of the magnetic field sensor is evaluated in the next section but spatial resolution of the device can be determined by taking into account

the arguments given in this section. Namely, referring to Fig. 1, one can see that an external magnetic induction z-component B_z uniformly distributed in the rectangular parallelepiped LWX_{ch} is needed for a proper operation of the HSDMAGFET, with L, W, and X_{ch} being, respectively, the channel length, the channel (transistor) width, and

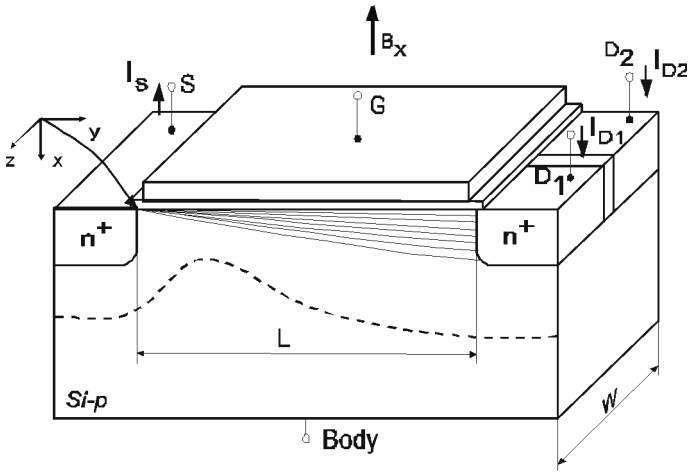

Fig. 4. A split-drain MAGFET structure after [3], [7], [8]

the channel thickness at the transistor drains. The channel thickness X_{ch} is close to an effective channel thickness d_{eff} that is defined in the next section and illustrated in Fig. 5, however, X_{ch} is always greater than d_{eff}, and is of the order of several hundreds of nanometers (d_{eff} depends on profile doping, depths of the drains, and thickness of the splitting insulator layer). The geometrical resolution of the HSDMAGFET in xy-plane is determined by LX_{ch}, and can be very high, making the device very suitable for reading high-density magnetically-encoded data (in the case of a standard SDMAG-FET this parameter equals LW, which is a much worse result).

3. Sensitivity of the HSDMAGFET

The relative magnetic sensitivity S [%/T] of the split-drain devices at small magnetic induction is defined as follows [3]:

$$S = \left| I_S^{-1} \frac{\partial \left(I_{D1} - I_{D2} \right)}{\partial B_z} \right|_{B_z = 0} \tag{3}$$

i.e., the partial derivative of the relative current imbalance with respect to the magnetic induction, taken at zero induction, which, for small B_z, can be replaced by [7, 9]

$$S = \left| \frac{I_{D1} - I_{D2}}{(I_{D1} + I_{D2}) B_z} \right| \tag{4}$$

Due to horizontally split drain design requirements, manufacturing the device needs a modified CMOS technology. The experimental research in this direction has not been undertaken so far. However, based on results of the work [9], we are able to estimate the predicted magnetic sensitivity of the device.

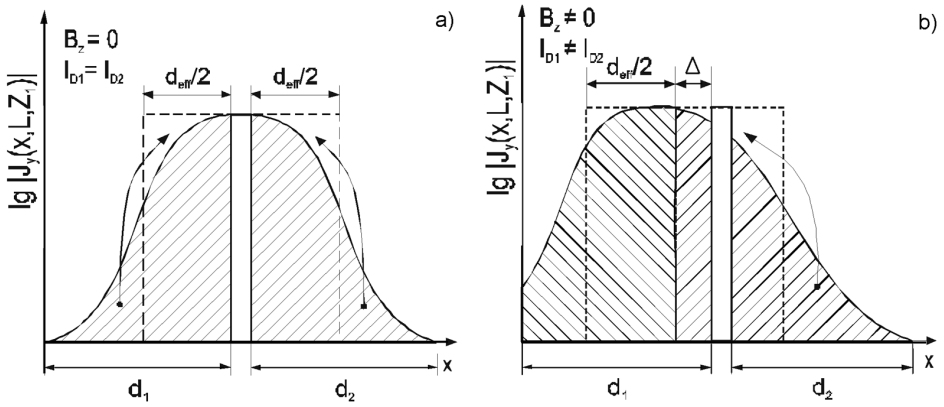

Fig. 5. An idealized current density distribution in a near-drain cross section of the channel of an HSDMAGFET operating in the saturation region of the output characteristics: a) $B_z = 0$, b) $B_z \neq 0$. The arrows show a method of calculating the effective near-drain channel thickness d_{eff}, where d_1 and d_2 are the thicknesses of the drains D_1 and D_2, respectively

Let us consider an idealized picture of the current density y-component distribution $J_y(x,L,z)$ in a near-drain cross section of an HSDMAGFET shown in Fig. 5a. In general, channel direct current I_{ch} through an arbitrary surface A perpendicular to the drawing plane in the transistor channel region can be expressed by

$$I_{ch} = -q \iint_A n(x,y)\, \mathbf{v}(x,y) dA \tag{5}$$

where q is the electronic charge, $n(x,z)$ – electron density distribution in xz-plane (Fig. 1), and $\mathbf{v}(x,z)$ – the velocity vector of electrons in the channel. Particularly, referring to Fig. 5a

$$I_{D1} = -W \int_0^{d_1} J_y(x,L) dx \tag{6}$$

and

$$I_{D2} = -W \int_{d_1+t_i}^{d_1+t_i+d_2} J_y(x,L) dx \tag{7}$$

Assuming that the velocity y-component $v_y(x,L)$ of current carriers (electrons) in appropriate regions of the plane $y = L$ is independent of x and equal to v_y (the longer the channel, the more adequate is the assumption), we can rewrite Eqs. (6) and (7) in the form:

$$I_{D1} = q\, v_y\, W \int_0^{d_1} n(x,L)\, dx \tag{8}$$

$$I_{D2} = q\, v_y\, W \int_{d_1+t_i}^{d_1+t_i+d_2} n(x,L)\, dx \tag{9}$$

Introducing an average current density in the neighbourhood of the splitting insulator, J_i, see Fig. 5(a),

$$J_i = \frac{J_y\left(d_1, L\right) + J_y\left(d_1 + t_i, L\right)}{2} \tag{10}$$

we can define an effective channel thickness at the HSDMAGFET drain, d_{eff}, as

$$d_{\text{eff}} = \frac{\int_0^{d_1} J_y(x,L)dx + \int_{d_1+t_i}^{d_1+t_i+d_2} J_y(x,L)dx}{J_i} \tag{11}$$

Assuming again that velocity y-component $v_y(x,L)$ of current carriers in appropriate regions of the plane $y = L$ is independent of x, Eqs. (10) and (11) can be written in the form:

$$J_i = \frac{q\, v_y \left(n\left(d_1, L\right) + n\left(d_1 + t_i, L\right) \right)}{2} \tag{12}$$

$$d_{eff} = \frac{2\left(\int_0^{d_1} n(x,L)dx + \int_{d_1+t_i}^{d_1+t_i+d_2} n(x,L)dx \right)}{n\left(d_1, L\right) + n\left(d_1 + t_i, L\right)} \tag{13}$$

As an external magnetic field acts on the HSDMAGFET, the Lorentz force causes the current layers in the channel region to deflect up or down (Fig. 1), depending on the direction of B_z. Introducing after [9] an effective current line deflection Δ, measured at the MAGFET drains (Fig. 5b), and defined as [9]

$$\Delta = L\, \mu_n \left| B_z \right| \tag{14}$$

where μ_n is the electron mobility in the channel, we can calculate the drain current imbalance, $\Delta I = I_{D1} - I_{D2}$ produced by magnetic field z-component B_z:

$$|\Delta I| = |I_{D1} - I_{D2}| = \frac{2 L \mu_n B_z}{d_{\text{eff}}} (I_{D1} + I_{D2}) \tag{15}$$

Inserting Eq. (15) into Eq. (4) and making use of Eqs. (12) and (13) lead to the relative sensitivity S [%/T] of the HSDMAGFET

$$S = \frac{2 \mu_n L}{d_{\text{eff}}} \tag{16}$$

or, alternatively,

$$S = \frac{\mu_n L \left[n(d_1, L) + n(d_1 + t_i, L) \right]}{\int_0^{d_1} n(x, L)\, dx + \int_{d_1 + t_i}^{d_1 + t_i + d_2} n(x, L)\, dx} \tag{17}$$

The mobility μ_n in Eqs. (14)–(17) is an electric field dependent parameter and its dependence on the longitudinal electric field component in the channel can be described as follows [10]:

$$\mu_n = \frac{\mu_{n0}}{\left[1 + \left(\frac{E_0}{E_C} \right)^B \right]^{\frac{1}{B}}}, \qquad E_0 = \frac{V_{DS}}{L} \tag{18}$$

where μ_{n0}, E_C, and B are low-field mobility, characteristic electric field, and a parameter ($1 \leq B \leq 5$), respectively.

From Eq. (17) it follows that the relative sensitivity S reaches its maximum value when the current carrier concentration at the cross-section plane for $y = L$ gets its maximum in the neighbourhood of the splitting insulator. This result converges well with the experimental results obtained for standard SDMAGFETs [7, 9].

Based on the theoretical analysis outlined in this section, and also on the results of numerical simulation (Fig 3b), we can estimate the expected sensitivity of the proposed HSDMAGFET. Taking some additional realistic data: μ_{n0} = 1000 cm^2·V^{-1}·s^{-1}, $E_C = 10^3$ V·cm^{-1}, B = 2, L = 10 μm, V_{DS} = 9.2 V, the calculated sensitivity value can reach 100 %/T, that is 50 times more than the experimental value 2–3 %/T obtained for a standard SDMAGFET [3, 7–9]. Again, examination of Eq. (17) allows us to speculate that even higher values of the sensitivity could be obtained for a more advanced design of the HSDMAGFET. Such a design should provide possibility for the drain current balance, $I_{D1} = I_{D2}$, at very low drain bias voltage V_{DS}, i.e., in the linear region of operation where the mobility value lowering is negligible.

4. A novel device related to the HSDMAGFET

Unlike the known SDMAGFET, the HSDMAGFET put forward in this work is sensitive to the *z*-component of the magnetic field enabling us to develop new types of semiconductor devices. An interesting example is discussed in this chapter.

A novel semiconductor device related to the HSDMAGFET, horizontally-split -drain current controlled field effect transistor (HSDCCFET) with two control electrodes has been proposed [11]. For the sake of brevity, the device can be called a CCFET. Operating principle of the proposed transistor is based on one of the galvanomagnetic phenomena, the Biot–Savart–Laplace law and the gradual channel detachment effect (GCDE).

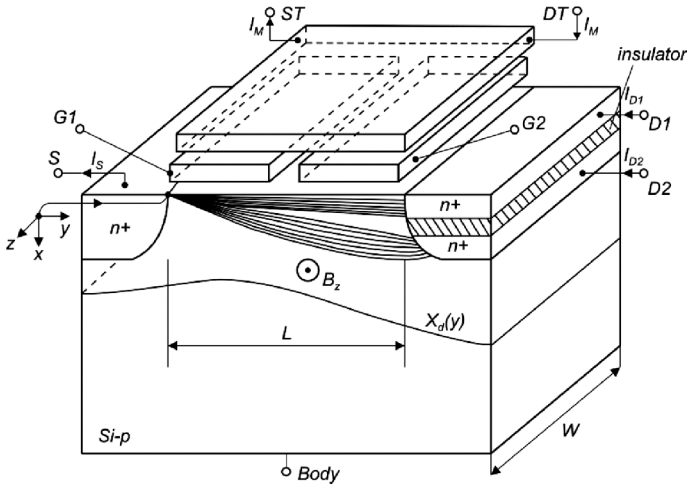

Fig. 6. Basic structure of the new current-controlled field effect transistor (CCFET)

If a dc current I_M flows between the terminals *DT* and *ST* of a conducting layer insulated from the transistor gates (Fig. 6), a magnetic field B_z is induced. According to the Biot–Savart–Laplace law, the magnetic induction B_z at any arbitrary point in the transistor channel is directly proportional to the current I_M. The magnetic field leads to an asymmetry in the terminal drain currents, which is a measure of the magnitude of the current I_M. An imbalance between the drain currents, defined as $\Delta I = I_{D1} - I_{D2}$, is a function of the transistor channel width W, channel length L, biasing voltages V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, and the current I_M which can be expressed as [1, 3, 7–9]:

$$\Delta I = I_{D1} - I_{D2} = f(W, L, V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, I_M) \tag{19}$$

Thus we can say that the novel transistor is a sensor of the current I_M which can flow in an arbitrary loop or branch of the integrated circuit (IC). In other words, the transistor is able to convert the current I_M flowing through an arbitrarily chosen connecting path in the IC into the difference between the drain currents, I_{D1} - I_{D2}. Like

a MOSFET, the CCFET has three primary regions of operation: cutoff, linear, and saturation. What is more interesting, the transistor is powerless-controlled, i.e., there is no voltage drop between the terminals *DT* and *ST*.

A p-channel version of the CCFET can be fabricated by reversing the polarities of the n- and p-type regions in Fig. 6. The direction of currents in the p-channel is opposite to that of the n-channel device, and the polarities of the operating bias voltages are reversed. The circuit symbols for n- and p-channel CCFETs are proposed in Fig. 7.

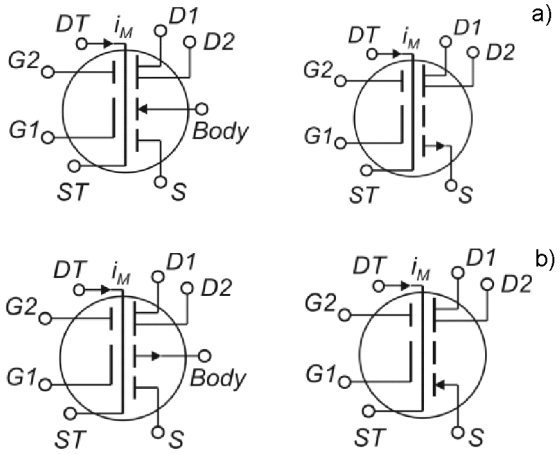

Fig. 7. Circuit symbols of the current-controlled field effect transistor (CCFET): a) for an n-channel device, b) for a p-channel device

In general, the device presented in this section can be applied as a magnetic field sensor and as an element of building blocks of integrated circuits (ICs). Selected basic circuit applications of the CCFET discussed in [11] include a current-controlled amplifier, operational current amplifier, and voltage–current multiplier cell.

An important feature of the device is that it can be controlled by the voltage V_{GS1} and the current I_M. Due to the principle of operation, power absorbed at input terminals *DT-ST* (Fig. 6) equals zero, hence the current I_M, or a fraction of it, can control a large number of such devices. Since a connecting path drawing the current I_M, isolated from the transistor structure, can be at an arbitrary potential, we can say that the CCFET can realize a function of a potential-free current detector (PFCD) or a potential-free current amplifier (PFCA). This feature of the device enables designers to eliminate transformers in IC design.

5. Conclusions

A novel MAGFET sensor structure with horizontally split drains has been put forward. Using analytical and numerical simulation approach, it was shown that predicted magnetic sensitivity of the sensor can reachthe value, to date unmatched, of

100 %/T. Therefore, HSDMAGFETs are very interesting for applications in magnetometry and reading high density magnetically encoded data. Also, a novel semiconductor device based on the HSDMAGFET concept, viz., horizontally-split-drain current controlled field effect transistor (HSDCCFET) with two control electrodes has been discussed. The new FET structure seems to be very promising for applications as a part of basic building blocks of integrated circuits. However, in both presented devices a modification of the standard CMOS technology is needed and remains crucial for the wider development of various magnetic field sensors based on the HSDMAGFET. One of possible further research directions is switching to III-V semiconductors and MAGFET sensors based on MESFET devices which benefits in higher carrier mobilities and possibility of epitaxial nano-layers bandgap engineering.

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