

Analysis of electrical equivalent circuit of metal–insulator–semiconductor structure based on admittance measurements

S. KOCHOWSKI¹, M. SZYDŁOWSKI^{1*}, R. PASZKIEWICZ², B. PASZKIEWICZ²

¹Institute of Physics, Silesian University of Technology, ul. Krzywoustego 2, 44-100 Gliwice, Poland

²Wrocław University of Technology, Faculty of Microsystem Electronics and Photonics,
ul. Janiszewskiego 11–17, 50-372 Wrocław, Poland

An electrical equivalent circuit of Al–(thermal)SiO₂–(n)Si structure has been proposed and the results of analysis of circuit parameters have been compared with classical methods of investigations of metal–insulator–semiconductor (MIS) structures. The electrical equivalent circuit of the structure contains constant phase elements. The analysis of admittance in terms of frequency characteristics was performed for broad range of biases from inversion to accumulation. The parameters of MIS equivalent circuit determined from impedance spectroscopy data are in good agreement with values obtained by the classical analysis of capacitance–voltage and conductance–voltage characteristics as well as the conductance method.

Key words: impedance spectroscopy; metal–insulator–semiconductor structure; constant phase element; electrical properties; silicon

1. Introduction

Development of modern electronic technologies is determined by new semiconductor materials which make the integrated devices possible to work in broad ranges of frequencies and temperatures. The analysis of such modern materials requires applying various methods. Measurements and analysis of electrical characteristics of metal–insulator–semiconductor (MIS) structures are useful tools for investigation of various semiconductor materials. Impedance spectroscopy [1] is one of the methods of analysis of electrical admittance characteristics.

In recent years, we discussed the usability of impedance spectroscopy to characterize electron processes in the MIS structures made of gallium arsenide [2–4] and

*Corresponding author, e-mail: michal.szydowski@polsl.pl

silicon [5]. The applied MIS electrical equivalent circuit included constant phase element (CPE) which made possible to describe frequency dispersion phenomena occurring in these systems. The CPE element has the admittance $Y_{\text{CPE}} = Q(i\omega)^n$, where Q and n are frequency independent parameters. For a further estimation of usability of the method, the impedance spectroscopy analysis should be performed for systems which could be easily investigated by the classical methods of analysis of electrical characteristics.

Al-(thermal)SiO₂-(n)Si structures were the object of our investigations. We proposed an electrical equivalent circuit of MIS structure describing the frequency dispersion of admittance characteristics in a broad range of signal frequencies and gate voltages from inversion to accumulation. The analysis of admittance in terms of frequency characteristics was performed using impedance spectroscopy and by the classic conductance method. We have also estimated basic parameters of investigated structures from the analysis of capacitance–voltage and conductance–voltage characteristics. The results of calculated curves fitting to experimental admittance data have been presented and some parameters of the equivalent circuit were related to values obtained by the conductance method.

2. Experimental

The investigations have been performed on Al–SiO₂–Si structures with 103±7 nm SiO₂ dielectric layer obtained by the thermal oxidation at 1150 °C under dry O₂ atmosphere on n-type (111) Si wafers of the resistivity of 1.5 Ω·cm. Before oxidation, silicon wafers were cleaned according to the standard procedure [6]. 0.5 μm thick gate electrodes of 1 mm in diameter were deposited by thermal evaporation of aluminum and photolithography successively. Aluminum layer was also used as a back ohmic contact to Si.

The measurements of the electrical characteristics have been done with a 4192A Hewlett Packard HF/LF impedance analyser working in a parallel circuit mode. The ac signal amplitude was kept at the value of 30 mV. The MIS capacitance and conductance versus bias (from –30 V to 10 V) at 1 MHz frequency as well as the MIS admittance versus frequency (from 500 Hz to 13 MHz) at a fixed bias (between –20 V and 10 V) have been recorded at room temperature.

3. Results and discussion

Figure 1 shows typical dependences of high frequency capacitance C and conductance G on bias U_g obtained at 1 MHz ac signal for the structures polarized from the inversion to the accumulation. According to Jakubowski et al. [7] and Witeczak et al. [8] we have estimated the insulator capacitance $C_{\text{OX}} = 286 \pm 2$ pF, MIS serial resistance $R_s = 13.1 \pm 0.5$ Ω and the Fermi level position in the bulk of semiconductor $u_b = 12.8 \pm 0.1$. Taking advantage of Ovsyuk [9] formulas, we used C_{OX} and u_b values to calculate theoretical dependence of space charge layer capacitance C_{SC} on the sur-

face potential v_s and of high frequency structure capacitance on the surface potential. The latter curve was used to plot (Fig. 1a (inset)) experimental dependence of surface potential v_s on bias U_g constructed by comparing experimental high frequency $C-U_g$ characteristics with calculated theoretical $C-v_s$ curve [10].

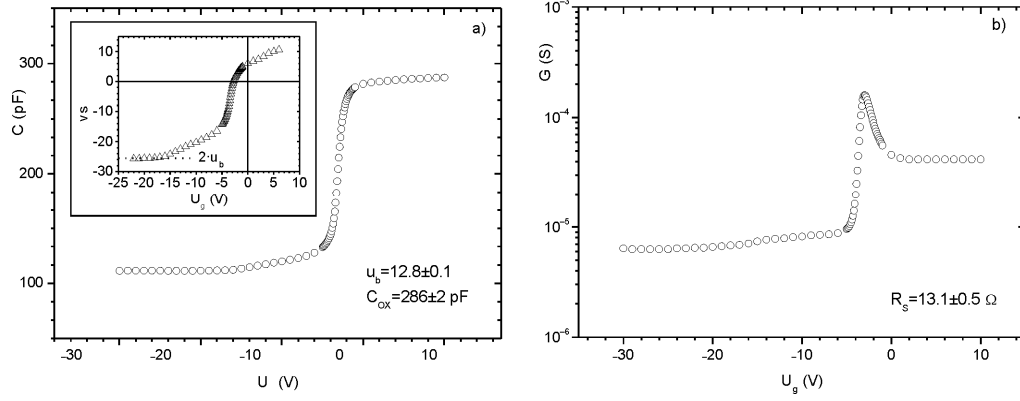


Fig. 1. Experimental $C-U_g$ (a) and $G-U_g$ (b) characteristics of Al–(thermal)SiO₂–(n)Si structure recorded at $f = 1$ MHz. The MIS structure was kept at 300 K. The inset shows the plot v_s vs. bias U_g constructed by comparing experimental high frequency $C-U_g$ characteristic with calculated theoretical $C-v_s$ curve [10].

The MIS capacitance C_{OX} as a $C-U_g$ maximum was determined from the characteristics, the Fermi level u_b calculated according to [7] and serial resistance R_s evaluated using formulas from [8]

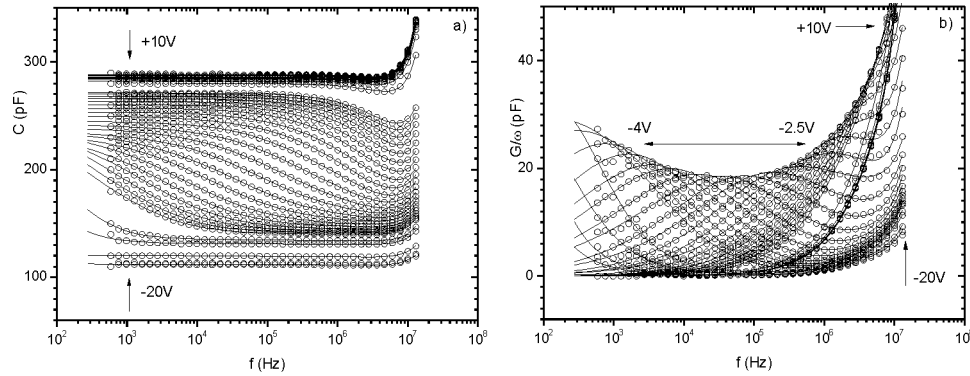


Fig. 2. Capacitance C and normalized conductance $G\omega^{-1}$ vs. frequency of Al–(thermal)SiO₂–(n)Si structures at various biases ($f = \omega/2\pi$). The sample kept at 300 K. Symbols represent experimental data while full lines are the best fits of experimental data using the circuits from Fig. 3.

In Fig. b) one can see characteristic maxima of normalized conductance corresponding to frequency dispersion of capacitance in Fig. a) (biases from -4 V to -2.5 V)

In Figure 2, we present experimental dependences of MIS capacitance and normalized conductance $G\omega^{-1}$ on frequency measured at a fixed gate voltage. It is visible that changes of the capacitance and conductance take place over a wide frequency range. The normalized conductance $G\omega^{-1}$ peaks, whose frequency depends on the gate

voltage, occur and the capacitance dispersion exists in the frequency range where these maxima are observed. We managed to describe the determined characteristics by equivalent circuits presented in Fig. 3. These circuits contain: insulator capacitance C_{OX} , serial resistance R_s , circuit inductance L , bias-dependent space charge layer capacitance C_{SC} , additional bias-dependent capacitance C_D , two constant phase elements $CPE_{1,2}$ characterized by $Q_{1,2}$ and $n_{1,2}$ parameters, and resistors $R_{1,2}$. The electrical equivalent circuit of the MIS structure simplifies for bias range $U_g < -5$ V (towards structure inversion, Fig. 3a) and $U_g > -3$ V (towards structure accumulation, Fig. 3c) while for $-5 \text{ V} \leq U_g \leq -3$ V (structure depletion) the circuit contains all elements (Fig. 3b).

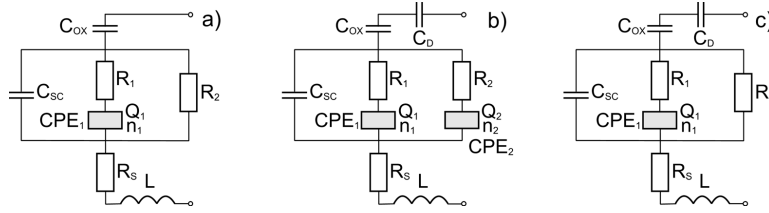


Fig. 3. Electrical equivalent circuits of the MIS structure for various bias ranges:

a) $U_g < -5$ V, b) $-5 \text{ V} \leq U_g \leq -3$ V, c) $U_g > -3$ V, C_{OX} – insulator capacitance, R_s – serial resistance, L – circuit inductance, C_{SC} – bias-dependent space charge layer capacitance, C_D – additional bias-dependent capacitance, $CPE_{1,2}$ – constant phase elements characterized by $Q_{1,2}$ and $n_{1,2}$ parameters, $R_{1,2}$ – resistances

The estimation of the equivalent circuit parameters was performed by the Levenberg–Marquardt algorithm [11] of simultaneous fitting of capacitance and normalized conductance curves to experimental data using the OriginLab software. The best fitted values of the equivalent circuit parameters are presented in Fig. 4 and the theoretical dependences calculated for these data are shown as full lines in Fig. 2. From the data presented in Fig. 4, one can see that the frequency behaviour of the investigated structures is very well reproduced by the proposed equivalent circuits in a full range of measured biases. Good fitting of theoretical dependences to the experimental data (Fig. 2) as well as the monotonous dependence of the circuit parameters on the gate voltage (Fig. 4) suggest that the elements of the equivalent circuit reasonably represent physical processes in various parts of the investigated structures. The values of insulator capacitance C_{OX} and serial resistance R_s are, as expected, practically bias independent being in very good agreement with the results obtained from $C-U_g$ and $G-U_g$ characteristics (Fig. 4). The serial resistance can arise from different sources [12], the main one being the resistances of the semiconductor material as well as of the contacts and electrical connections. The value of the circuit inductance parameter L equals $0.12 \pm 0.02 \mu\text{H}$, and is negligibly small and bias independent. The origin of the additional bias-dependent capacitance C_D is not clear at the moment. However, regarding this parameter made it possible to obtain monotonous dependence of C_{OX} capacitance on the gate voltage and its compatibility with the value obtained from the capacitance

–voltage characteristic. The estimated space charge layer capacitance C_{SC} coincides with theoretical C_{SC} curve calculated based on the u_b value determined from $C-U_g$ characteristics for biases corresponding to inversion and depletion region of MIS structure (Fig. 4a). The essential features of the admittance characteristics of the MIS structures are described by the constant phase elements CPE_1 and CPE_2 connected in series with resistors R_1 and R_2 , respectively.

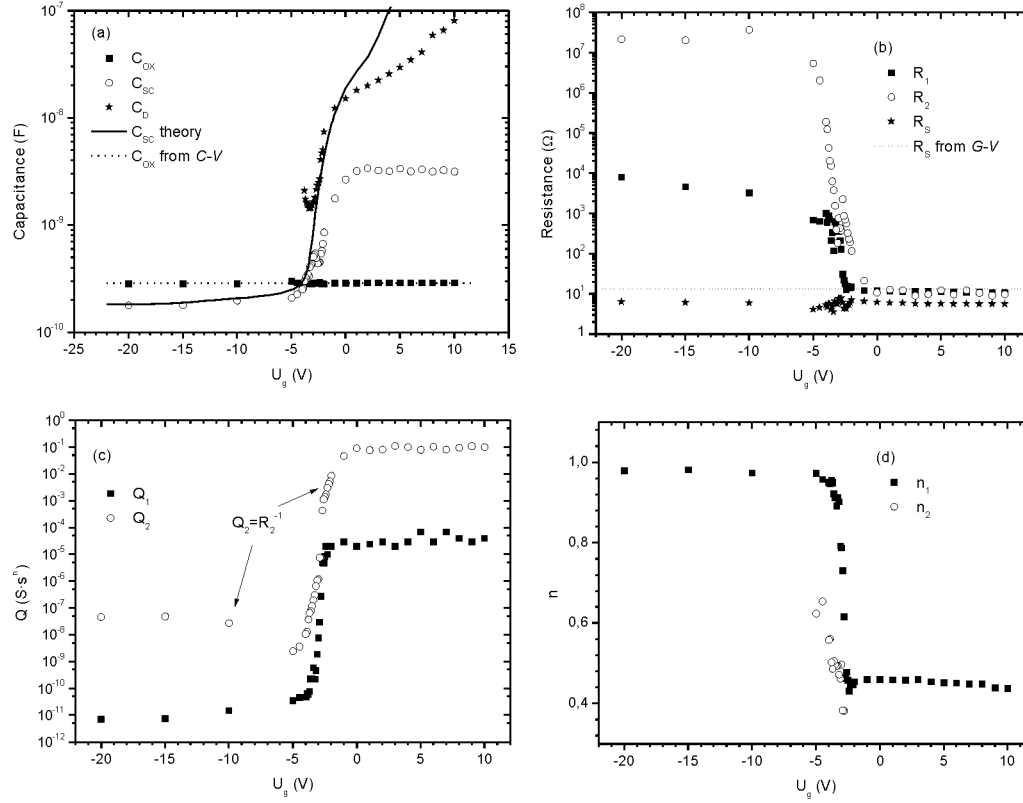


Fig. 4. Values of equivalent circuit parameters from Fig. 3 obtained at various biases U_g (symbols): a) C_{ox} —insulator capacitance, C_{sc} —bias-dependent space charge layer capacitance, C_d —additional bias-dependent capacitance; b) R_1 and R_2 resistances, R_s serial resistance; c) constant phase element parameters Q_1 , Q_2 and parallel resistance $R_2=Q_2^{-1}$; d) constant phase elements parameters n_1 and n_2 . Dashed line in (a) represents constant insulator capacitance C_{ox} obtained from $C-U_g$ characteristics. Full line in a) shows a theoretical curve of space charge layer capacitance C_{sc} vs. bias calculated according to Ovsyuk formulas [9] where the surface potential ψ_s was assigned to U_g using inset in Fig. 1a. Dotted line in b) represents constant serial resistance R_s obtained from $G-V$ characteristics according to [8]

They are related to electron processes with a broad distribution of time constants around the characteristic values $\tau_1 = (R_1 Q_1)^{1/n_1}$ and $\tau_2 = (R_2 Q_2)^{1/n_2}$. The time constants were calculated using data from Fig. 4b, c, d and are presented in Fig. 5. We also used the Nicollian–Goetzberger–Lopez conductance method [13] to extract time constants

τ_{NGL} from measured normalized conductance in depletion. These time constants characterize exchange of electrons between SiO_2 –Si interface and semiconductor states. The τ_{NGL} values, presented in Fig. 5, are in very good agreement with τ_2 values. This suggests that time constants τ_2 and τ_{NGL} are connected with the same electron process. Thus the constant phase element CPE_2 in series with R_2 resistance describes the dispersion phenomena evoked by the semiconductor–insulator interface states. The time constant τ_1 is practically gate voltage independent. This kind of behaviour points to the presence of the deep traps in the semiconductor space charge region. The CPE_1 element with the parameter $n_1 = 0.95$ for $U_g < -5$ V ($v_s < -13$, see Fig. 1) has “capacitive” character (for pure capacitance $n = 1$) and together with R_1 resistance they characterize the time constant of monoenergetic electron traps in a lower part of the energy gap of the semiconductor. For $U_g > -3$ V ($v_s > 0$), what corresponds to the traps located in an upper part of the energy gap; the CPE_1 element with the parameter $n_1 = 0.46$ connected with R_1 resistance describes electron processes with a broad spectrum of time constants.

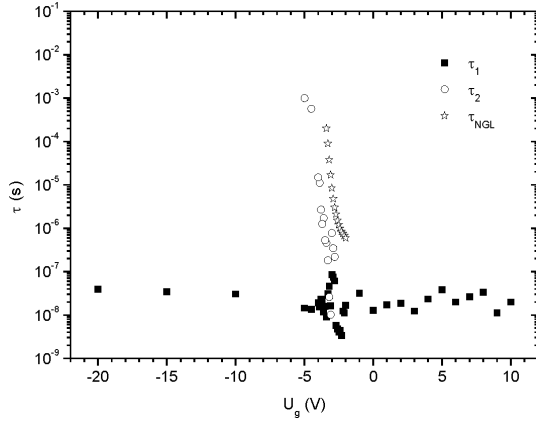


Fig. 5. Time constants τ at various biases U_g ; τ_1 and τ_2 were calculated from Q_1 , n_1 , R_1 and Q_2 , n_2 , R_2 data presented in Fig. 4b–d. Time constant τ_{NGL} was estimated according to Nicollan–Goetzberger–Lopez method [13]

The presented results show that the proposed equivalent circuits with constant phase elements allow one to describe complex processes evoked by localized electron states in the MIS structures, pointing to the usability of the impedance spectroscopy method for the analysis of other materials and systems, especially where standard methods are difficult or impossible to apply.

4. Conclusions

We proposed the electrical equivalent circuit of Al–(thermal) SiO_2 –(n)Si structure with constant phase elements describing frequency behaviour of admittance characteristics in a broad range of gate voltages and frequencies. The parameters of MIS equivalent circuit determined by the impedance spectroscopy method are in good agreement with the values obtained by the standard analysis of admittance–voltage

characteristics as well as the conductance method. The constant phase elements in series with resistances describe electron processes connected with localized electron states resulting in frequency dispersion of measured characteristics of structures.

Acknowledgements

The authors wish to thank Prof. Karol Nitsch from Wrocław University of Technology, Faculty of Microsystem Electronics and Photonics, for providing the samples and for many valuable discussions.

References

- [1] MACDONALD J.R., *Impedance Spectroscopy*, Wiley, New York, 1987.
- [2] KOCHOWSKI S., NITSCH K., *Thin Solid Films*, 415 (2002), 133.
- [3] KOCHOWSKI S., NITSCH K., PASZKIEWICZ B., PASZKIEWICZ R., *Thin Solid Films*, 444 (2003), 208.
- [4] KOCHOWSKI S., NITSCH K., PASZKIEWICZ B., PASZKIEWICZ R., SZYDŁOWSKI M., *Appl. Surf. Sci.*, 235 (2004), 389.
- [5] KOCHOWSKI S., SZYDŁOWSKI M., *Zesz.Nauk. Pol. Śląskiej, Ser. Mat.-Fiz.*, 91 (2004), 199.
- [6] *Model Laboratory Processes and Procedures*, Bell Telephone Laboratories, New Jersey, 1965.
- [7] JAKUBOWSKI A., INIEWSKI K., *Solid-State Electron.*, 26 (1983), 755.
- [8] WITCZAK S.C., SUEHLE J.S., GAITAN M., *Solid-State Electron.*, 35 (1992), 345.
- [9] OVSYUK V.N., *Electron Processes in Semiconductors with Space-Charge Region*, Nauka, Novosibirsk, 1984 (in Russian).
- [10] TERMAN L.M., *Solid-State Electron.*, 5 (1962), 285
- [11] PRESS W.H., TEUKOLSKY S.A., VETTERLING W.T., FLANNERY B.P., *Numerical Recipes in C. The Art of Scientific Computing*, Cambridge University Press, Cambridge, 2002.
- [12] NICOLLIAN E.H., BREWS J.R., *MOS (Metal-Oxide-Semiconductor) Physics and Technology*, Wiley, New Jersey, 2003.
- [13] NICOLLIAN E. H., GOETZBERGER A., LOPEZ A.D., *Solid-State Electron.*, 12 (1969), 937.

Received 28 April 2007
Revised 16 February 2008