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Optimization of MFIS structures containing poly(vinylidene-fluoride trifluoroethylene) for non-volatile memory applications

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In the paper, we report on ways to optimize metal–ferroelectric–insulator–semiconductor (MFIS) stacks in terms of the thickness combination of the ferroelectric and the buffering insulator layers in order to reduce the operation voltage of MFIS based non-volatile memory elements. The stack contains poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) as a ferroelectric layer. We discuss the optimization of the deposition of this material in order to produce thin films with high polarization. This must be accompanied by an adapted buffer layer, where reduction of thickness as well as increase of permittivity can be taken into account. We show the results based on capacitance voltage measurements (CV) on MFIS stacks, where SiO_2 and Al_2O_3 of different thicknesses have been used. Furthermore, we perform simulations of the CV characteristics and we are able to quantify the polarization and decline it from the CV curves. We observe for a 120 nm P(VDF-TrFE)/11 nm Al_2O_3 stack in a ±20V CV loop almost saturated polarization values as predicted by the simulations in that way.

Keywords: *P*(*VDF-TrFE*)*, MFIS, non-volatile memory, FeFET*

1. Introduction

Ferroelectric field effect transistors (FeFETs) are considered candidates for future non-volatile and non-destructive readout memory cells [1, 2]. The first attempt of combining the ferroelectricity with a field effect device has been demonstrated in [3]. The physics of the FeFET is described in [4]. The working principle of the device is based on bistable influence of different polarization states inside the ferroelectric insulator on the drain current (refer to Fig. 1a). The substitution of conventional perowskite type ferroelectrics by a polymer type material leads to possible low cost solutions of this kind of a memory cell. Furthermore, FeFETs composed of conven-

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tional materials have been shown to work in general but they need expensive high temperature and high oxygen partial pressure processing steps inducing also unintentional and undefined interfacial layers [2, 5]. Poly(vinylidene fluoride trifluoroethylene) P(VDF-TrFE) is an organic ferroelectric material. It is available for spin coating at room temperature after solving it in non-toxic 2-butanone. In this case, the substrates can have well defined buffer layers. The properties of P(VDF-TrFE) have extensively been reviewed in [6]. Recently, attempts at realizing organic FeFETs using P(VDF-TrFE) have been reported [7–9].

In this paper, we will mainly focus on steps to further improve the characteristic of metal–ferroelectric–insulator–semiconductor (MFIS) structures, which contain P(VDF -TrFE) as ferroelectric layers. Comparisons of results of measurements with predictions based on a simulation procedure proposed by Miller and McWorther [4] are discussed. We investigate the preparation procedure of the polymer layer as well as the influence of the buffer layer. We perform capacitance–voltage (CV) measurements on MFIS based structures. Due to the dipole switching of the P(VDF-TrFE) chains, the CV curves show a hysteresis [4] (refer to Fig. 1b), which depends on the maximum applied voltage in the CV loops [9], i.e. on the polarization of the ferroelectric material.

2. Experimental

Preparation. As a copolymer, we use P(VDF-TrFE) in a molar ratio of 70/30. The material was delivered as a film from Piezotech S.A., France. The film was solved in 2-butanone and spin coated onto the substrates. The thickness of the polymer film can be varied considerably, depending on the velocity and the concentration of the solution, as discussed in the results section. Annealing was performed for 2 h at 135 °C, and, for comparison also, samples without annealing were prepared. The thicknesses of the spin coated films were measured with a Taylor–Hobson profilometer (Talystep).

For electrical characterization, MFIS capacitors were fabricated on silicon p-type substrates with (100) orientation and the resistivity 1–20 Ω·cm. As buffer layer, 10–235 nm SiO_2 or 11 nm Al_2O_3 was used. As a top electrode, aluminum was used, which was thermally evaporated through a shadow mask with diameters between 500 μm and 900 μm. The set-up of a MFIS capacitor is shown in Fig. 1b.

The CV measurements were carried out with a LCR-Meter Agilent 4284A at the frequency of 1 MHz with a sweep of 0.1 V/s. Measurements at higher temperatures were performed keeping the sample holder in a common drying oven. All measurements were started in accumulation (negative gate bias) and finished there too, after driving the voltage in the investigated range to inversion and backwards (e.g., from –10 V to 10 V and back again to –10 V, we call this a "±10 V loop", for short). Other intermediate measurements were taken while driving the voltage over the investigated range in a "voltage loop" (e.g. , from –10 V to 10 V and back again).

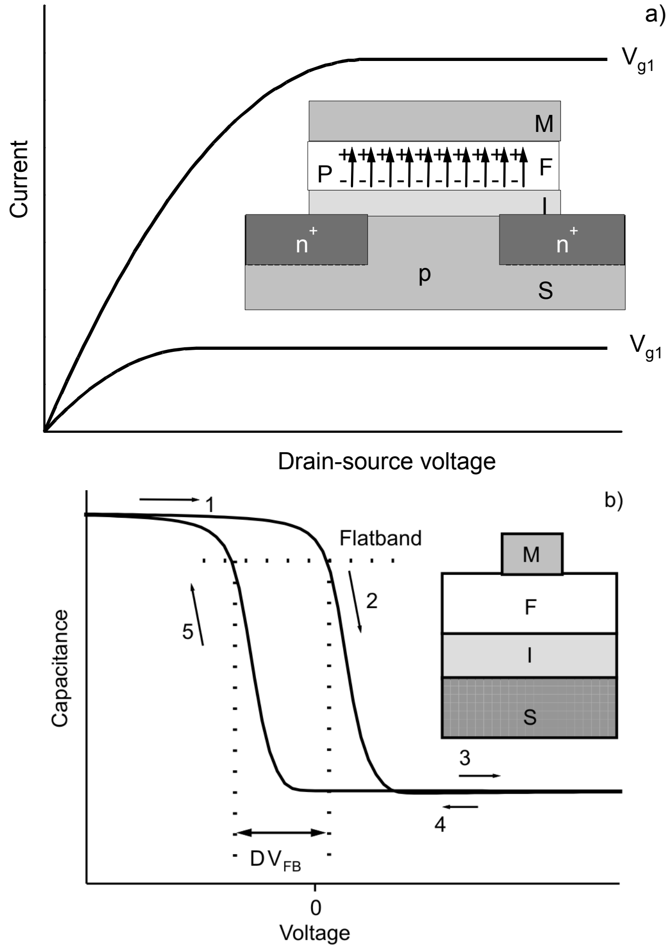

Fig. 1. Set-up and output characteristic of a FeFET. Due to switching of the dipoles after the programming, the current is showing two different states at the same gate voltage (a) as weel as set-up and CV characteristic of a MFIS capacitor (b), with a hysteresis caused by the polarization loop

Modulation. Miller and McWorther developed a method to include the ferroelectric polarization into the characteristics of FeFETs [4]. We use parts of it to model the CV characteristic of MFIS capacitors. The area capacitance of the MFIS system C''_{MFIS} can be written as follows:

$$\frac{1}{C''_{\mathrm{MFIS}}} = \frac{d_{\mathrm{PVDF}}}{\varepsilon_0 \varepsilon_{\mathrm{PVDF}}} + \frac{d_{\mathrm{buf}}}{\varepsilon_0 \varepsilon_{\mathrm{buf}}} + \frac{1}{C''_{\mathrm{S}}} = \frac{1}{C''_{\mathrm{stack}}} + \frac{1}{C''_{\mathrm{S}}} \tag{1}$$

where ε_0 is the permittivity of vacuum, $\varepsilon_{\mathrm{PVDF}}$ and $\varepsilon_{\mathrm{buf}}$ are the relative electric permittivities of the ferroelectric and the buffer layers, while d_{PVDF} and d_{buf} are their thick-

nesses. C''_S is the area depletion capacitance calculated from the derivative $d\sigma_S/d\phi_S$ of the semiconductor surface charge σ_S, which follows the same function of the silicon surface potential ϕ_S as that known for the CV characteristic of the MIS system[10]. The gate voltage V_g can then be written as

$$V_g = \phi_S - \frac{\sigma_S}{C''_{stack}} + V_{MS} - P(E_{PVDF}) \frac{d_{PVDF}}{\varepsilon_0 \varepsilon_{PVDF}} \tag{2}$$

where V_{MS} is the work function difference between metal and semiconductor, C''_{stack} is the insulator capacitance calculated by the two first terms in Eq. (1), and P is the dipole polarization, which depends on the electric field E_{PVDF}

$$E_{PVDF} = \frac{-[\sigma_S + P(E_{PVDF})]}{\varepsilon_0 \varepsilon_{PVDF}} \tag{3}$$

in the ferroelectric and its history. The saturated polarization hysteresis $P^{\pm}_{sat}$ is defined by

$$P^{\pm}_{sat} = \pm P_S \tanh\left[\frac{\pm E_{PVDF} - E_c}{2\Delta}\right] \tag{4}$$

where P_S is the spontaneous polarization (i.e., the saturation polarization), E_c is the coercive field and Δ is a hysteresis loop parameter, being a function of the ratio of the remanent and saturated polarization. The dipole polarization at step t is then calculated by a numerical integration using the data known at step $t - 1$:

$$P(E_{PVDF}(t)) = P(E_{PVDF}(t-1)) + \left[(E_{PVDF}(t) - E_{PVDF}(t-1)) \frac{d}{dE_{PVDF}} P(E_{PVDF}(t-1))\right] \tag{5}$$

The term $E_{PVDF}(t)$ is then eliminated by using Eq. (3). Furthermore, dP/dE_{PVDF} is a function of dP_{sat}/dE_{PVDF}, P_{sat}, P and P_S as:

$$\frac{dP^{\pm}}{dE_{PVDF}} = \left\{1 - \tanh\left[\sqrt{\frac{P - P_{sat}}{\xi P_S - P}}\right]\right\} \frac{dP^{\pm}_{sat}}{dE_{PVDF}} \quad \text{with} \quad \begin{matrix} \xi = 1 \quad \text{for} \quad \frac{dE_{PVDF}}{dt} > 0, \\ \xi = -1 \quad \text{for} \quad \frac{dE_{PVDF}}{dt} < 0 \end{matrix} \tag{6}$$

Knowing the actual polarization, the electric field E_{PVDF} and the gate voltage V_g can be determined from Eqs. (3) and (2), respectively, and the CV characteristic is given for every point of the loop. For further details refer to [4].

Data obtained by fitting methods which use this procedure will be shown in the paper. Additionally, we also use a simplified method to compare the results of measurements in a relative way being therefore more qualitative. As a value of the hystere-

sis of the CV loop we define the voltage window at flat band condition (ΔV_{FB}, refer to Fig. 1b), which is also called a memory window. Assuming, that this shift is caused by the dipole charges due to the polarization, ΔV_{FB} is then used to calculate the surface charge density N, which is a more qualitative value of the polarization

$$P \propto N = \frac{\Delta V_{\mathrm{FB}}\, \varepsilon_0 \varepsilon_{\mathrm{PVDF}}}{q d_{\mathrm{PVDF}}} \tag{7}$$

where q is the elementary charge.

3. Results and discussion

3.1. Phase transition

Here, we establish whether the CV hysteresis is or is not controlled by the bistable polarization and not by charges, which are injected into the buffer or the polymer layer. As a first test, we perform CV measurements of reference samples without P(VDF-TrFE) and do not observe any hysteresis. Then, CV loops at elevated temperatures are recorded and we find a decrease in the flatband voltage window, while the hysteresis totally vanishes at temperatures around 100 °C (Fig. 2a) indicating a phase transition from the ferroelectric to the paraelectric phase. In Figure 2b, this effect is shown for two samples of different P(VDF-TrFE) thicknesses on a 100 nm SiO_2/Si substrate. For both samples the flatband voltage shift is reduced to almost zero values at ca. 100 °C. Furthermore, by analyzing the accumulation capacitance of the CV loop we estimate the temperature dependence of the dielectric constant. For P(VDF-TrFE) with more than 50% VDF content, the phase transition was found to be of thermodynamically first order [6, 11]. A classical theory (Landau theory) delivers the Curie –Weiss law describing the temperature dependence of the reciprocal permittivity near first order transition [6, 11, 12] as

$$\frac{1}{\varepsilon'} \propto \frac{\pm(T_0 - T)}{C_i} \tag{8}$$

where the sign (±) is positive for temperatures lower than the phase transition temperature (the Curie temperature, $T < T_c$) and negative for temperatures above it ($T > T_c$). C_i are the Curie constants ($i = 1$ for $T < T_c$, $i = 2$ for $T > T_c$). T_0 is not exactly the Curie temperature [6, 12] and in the case of a first order transition it is smaller than T_c [12]. Figure 2c shows the temperature dependence of the reciprocal permittivity for the same samples as in Fig. 2b. From the slope of these plots we determine the values of C_1 of around 1000 K. This is in the same order of magnitude as in other papers [11, 13, 14], but our values are higher by a factor of 1.5 to 2. Here we have to state, that the permittivity disperses with the VDF content as well as with the frequency [6].

The CV loops are recorded at 1MHz, while the corresponding values published elsewhere [11, 13, 14] are observed at lower frequencies.

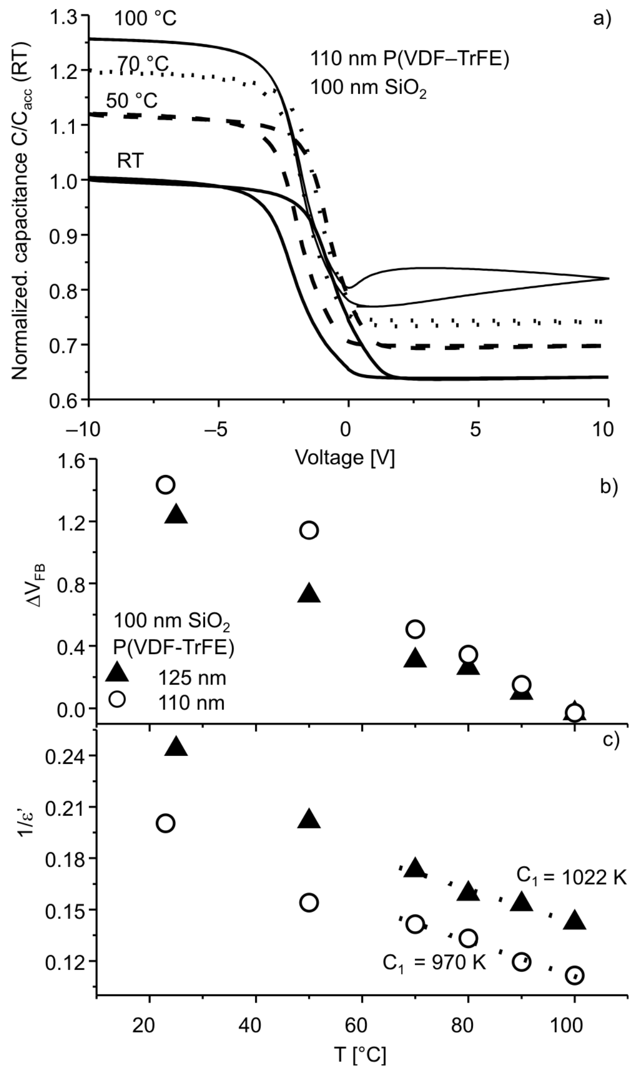

Fig. 2. CV curves of a 110 nm P(VDF-TrFE)/100nm SiO_2 stack at room temperature (RT) (a), the values of the capacitance are normalized to the accumulation capacitance (i.e. C_{Stack}) at room temperature; and flatband voltage shift (b) and the reciprocal permittivity (c) in dependence on temperature for a stack with 100 nm SiO_2 and 125 nm (filled triangle) or 110 nm (open circles) P(VDF-TrFE)

Furthermore, other VDF contents (52–55%, [11, 13, 14]) compared to our samples (70%) were used, and much thicker samples (11–100 μm in [13, 14]) have been analyzed. It was shown that the value of the C_1 constant increased as the layer thickness was reduced to 100 nm [11].

3.2. Optimization of the sample preparation

3.2.1. Polymer thickness, spin coating

In order to reduce the operation voltage of a memory device containing a P(VDF -TrFE) layer, due to its high coercive field (47–100 MV/m [6, 15]), the thickness of the ferroelectric layer should be downscaled below 100 nm.

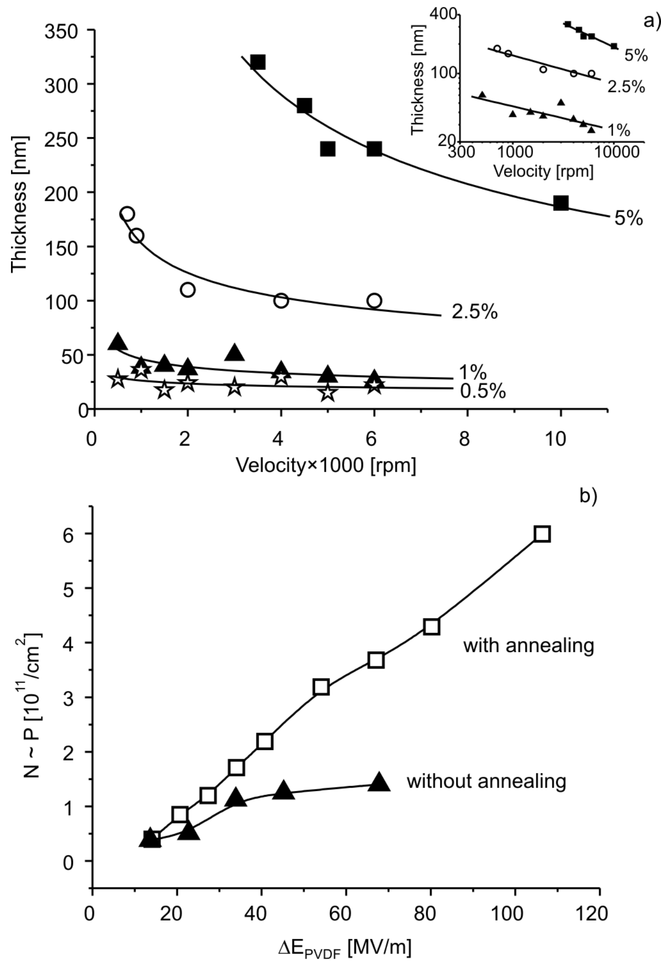

Fig. 3. Spin coating calibration of P(VDF-TrFE): thickness dependence on spin speed (a) at various solution concentrations. The inset depicts the log-log plot of the thickness versus the speed and dependence of the polarization proportional value *N* on the electric field loop (b) for one non-annealed sample (350 nm P(VDF-TrFE) and one annealed stack (220 nm P(VDF-TrFE)). Both layers were spun on a 235 nm SiO_2 buffer layer. The annealing was performed at 135 °C for 2 h

However, it should be noted that an increase of the coercive field of P(VDF-TrFE) with shrinking of the polymer thickness below 100 nm has been observed for this ma-

terial [6, 16]. Therefore, it should be possible to find an optimum solution for these two opposite trends. For that reason, it should be possible to adopt a wide range of applicable layer thickness.

In Figure 3a, the final film thickness versus the final spin speed is shown for various concentrations of the solution. In [17, 18] models for the spin coating have been developed, taking into account the solvent evaporation and a non-Newtonian character of the rheological behaviour of the resists. Jenekhe [18] introduced a parameter α, describing the influence of solvent evaporation on the viscosity of the fluid during spin coating. In a general dependence

$$d \propto w^{-p} \qquad \text{with} \qquad p = \frac{2}{2+a} \tag{9}$$

where d is the final thickness and ω is the angular frequency. By analyzing a log–log dependence of the thickness on the speed (inset of Fig. 3a) we determine mean values of p of 0.23 in the solution concentration range of 0.5–2.5%, while for the thicker solution of 5%, the value of 0.48 is found, which is in the typical range of 0.40–0.82 for resists discussed in [18]. Generally, we find an increased slope p by increasing the concentration of the solution. This is in good agreement with the modulations in the literature and is attributed to the increase in fluid viscosity and therefore to the more prominent non-Newtonian behaviour at higher concentrations [17].

With this calibrated spin coating procedure we are able to fabricate films in a wide range of thicknesses between 10 nm and 1 μm. Using it, we could recently identify interface reactions between aluminum electrodes and the P(VDF-TrFE) as the reason for decreased polarization values, when the polymer thickness is shrunk below 150 nm [15, 19]. Furthermore, we have recently shown that the ferroelectric switching shows still an extrinsic like behaviour in films as thin as 10 nm [20].

3.2.2. Annealing

We have already partially shown the effect of the annealing step on our CV measurements [21], where we find much more symmetric behaviour in the flatband voltage shift inside one CV loop after annealing. Conversely, the CV loops of non-annealed samples additionally shift due to a probable charge injection.

Here we analyze the impact of annealing to a higher polarization value. In Figure 3b, we show the dependence of N value – proportional to the polarization – calculated by Eq. (7) on the applied electrical field window of the CV loop for one annealed and one non-annealed sample. We observe much higher values of the polarizability for the annealed sample, while the non-annealed sample already shows saturation even here, where a thick SiO_2 buffer layer of 235 nm is used. In [6] a strong effect of annealing for improving the crystallinity of P(VDF-TrFE) was clearly discussed, which results in higher polarization values by a factor of 3 to 4. Our results are in good agreement with this finding.

3.3. Optimization of the buffer layer

As discussed above, a layer shrinking of the polymer is essential for a low voltage operation of a memory device based on MFIS like structures. However, in a MFIS stack a part of the programming voltage drops over the buffering insulator, which is necessary for the hindrance of depolarization, thereby causing leakage currents.

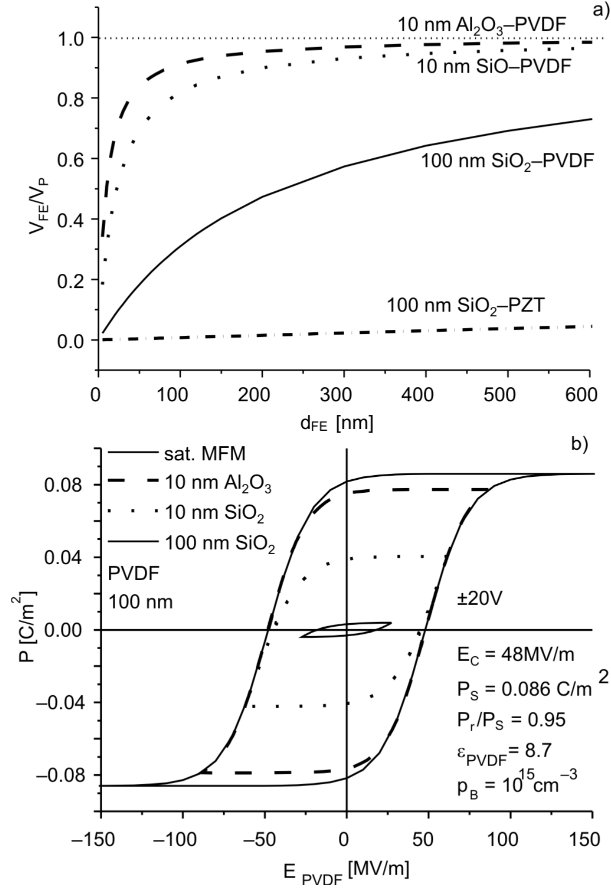

Fig. 4. Calculation of the ratio of the voltage over the ferroelectric layer V_{FE} and the applied voltage V_p in dependence on the ferroelectric thickness d_{FE} using Eq. (10) (a), and simulation of $P(E)$ curves of stacks with 100 nm P(VDF-TrFE) (b) for MFIS systems, which use various buffer layers: 100 nm SiO_2 (thick solid lines), 10 nm SiO_2 (dotted lines) and 10 nm Al_2O_3 (dashed lines). For comparison, results for a stack with a conventional PZT ferroelectric (dashed dotted line in part a) and for a MFM capacitor with the same thickness of the ferroelectric layer (thin solid line in part b) are shown. Because in part (a) PZT is used as a ferroelectric (FE) material as well, the plot shows the dependence of V_{FE}/V_P on d_{FE}, i.e. in Eq. (10) d_{PVDF}, $\varepsilon_{\text{PVDF}}$ and V_{PVDF} should be substituted by d_{FE}, ε_{FE} and V_{FE}

Again for a low voltage operation, these programming losses should be as small as possible. Furthermore, in the “off state” of the memory, the gate is normally grounded.

Due to charge neutrality, the electric field caused by the polarization of the ferroelectric layer will be neutralized by an established field in the buffer layer, leading to depolarization fields, which can corrupt the saved information [5]. This fact meets the same requirements as for the low voltage operation, where a high capacitance of the buffer layer and a moderate permittivity value of the ferroelectric material are needed. In the accumulation regime of the MFIS structure, the ratio of the voltage drop over the ferroelectric layer (V_{PVDF} respectively V_{FE}) to the programming voltage (write, V_p) can be estimated by a simple model of two capacitors in series, and the following formula can be used:

$$\frac{V_{PVDF}}{V_p} = \frac{1}{1 + \frac{\varepsilon_{PVDF}}{\varepsilon_{buf}} \frac{d_{buf}}{d_{PVDF}}} \tag{10}$$

As is shown in Fig. 4a, this ratio depends on the thickness of the ferroelectric layer. The thickness of the ferroelectric layer could be increased so that a high voltage ratio is attained but this contradicts the criteria for low voltage operation. In the opposite direction, this ratio is reduced by making the polymer layer thinner. Therefore, the buffer layer should be adapted either by the reduction of its thickness (dotted line in Fig. 4a) or by increasing its permittivity (dashed line in Fig. 4a). In addition, Fig. 4a depicts also, that for the case in which a buffer layer is needed (see Sect. Introduction), a ferroelectric with a relatively small permittivity is preferable in terms of this voltage divider optimization. In terms of optimization of the buffer layer, it should be also taken into account that the fully saturated regime of the polarization of the ferroelectric should be achieved preferably in order to get a stable working MFIS memory stack. However, this simple model of the voltage divider does not consider the polarization inside the ferroelectric layer. Hence, we performed also simulations of $P(E)$ curves using the procedure described in Sect. 2.2 with the same thickness of the buffer layer and materials as used in Fig. 4a (refer to Fig. 4b). Assuming, that ±20 V CV loops are performed, we calculate the resulting $P(E)$ loop for a 100 nm P(VDF-TrFE) layer with a buffer layer of 100 nm SiO_2, 10 nm SiO_2, or 10 nm Al_2O_3. For comparison, the saturation loop of a pure 100 nm thick P(VDF-TrFE) capacitor (metal –ferroelectric–metal, MFM) is shown in Fig. 4b as well. The values of Ec, Ps and ε_{PVDF} are given in the legend of Fig. 4b and are taken from our former results [15]. The assumed values of the relative dielectric constants of SiO_2 and Al_2O_3 were 3.9 and 9, respectively. We clearly observe that for this configuration and a CV loop of ±20V, a 10 nm Al_2O_3 buffer layer almost leads to a complete saturation. This is confirmed by the results of measurements shown in Fig. 5a. Here, again we show the more qualitative polarization value N in dependence of the maximum applied voltage of the CV loop. We observe a similar behaviour as predicted by the simulation, the stack with 11 nm Al_2O_3 buffer layer shows a much higher polarization value than the stack with almost the same SiO_2 thickness and here the ferroelectric seems to be already more or less in saturation. This means that even this simplified calculation of the N value delivers good qualitative information about the polarization.

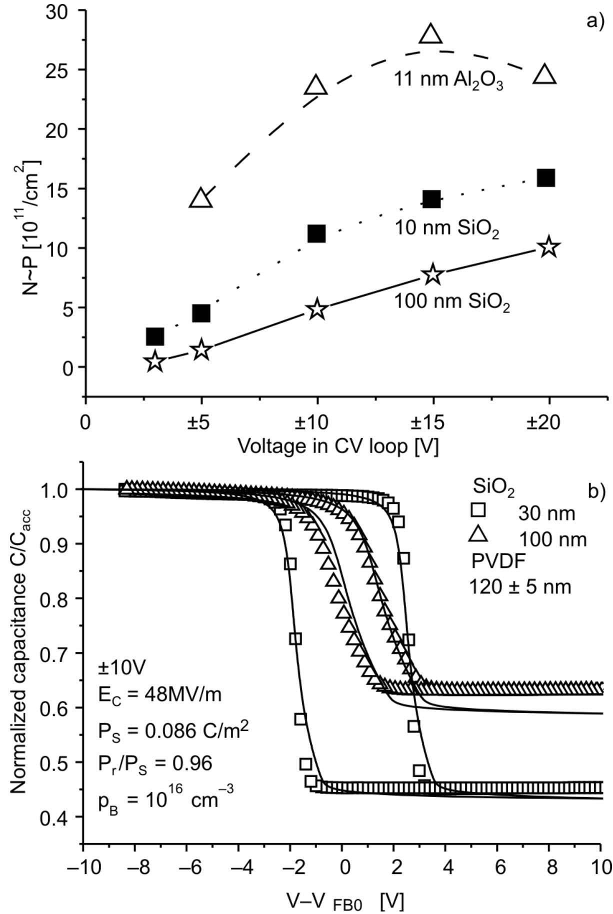

Fig. 5. Dependence of the polarization proportional value N on the maximal voltage applied in the CV loop (a) for MFIS stacks consisting of 120 nm P(VDF-TrFE) and 100 nm SiO_2, 10 nm SiO_2 or 11nm Al_2O_3 and measured (symbols) and calculated (lines) CV curves of stacks with 120 nm P(VDF-TrFE) and 30 nm or 100 nm SiO_2 (b). The values of the capacitance are normalized to the accumulation capacitance (i.e. C_{stack}) of each individual sample. The curves correspond to the initial flatband voltage (V_{FB0}) of every sample in order to visualize the hysteresis due to the ferroelectric switching more easy

To get more quantitative parameters of the polarization loop, the CV curve should be fitted to the model described above in Sect. 2.2. Here, we just show two examples of modelling, where a 120 nm P(VDF-TrFE) layer is combined with a 30 nm or 100 nm SiO_2 layer. In Figure 5b, the ±10V CV measurements on these stacks are marked by symbols, while the results of simulation are shown with solid lines. We use the same values as above for E_c, P_S and ε_{PVDF} (refer to the legend of Fig. 5b) as known values. The model is in very good agreement with the measurement. For a real fitting procedure the E_c and P_S values as well as the ratio of the remanent and saturated polarization should be adapted.

4. Conclusion

Ways to optimize a MFIS stack have been described. The optimization of a sequence of layer thickness of the ferroelectric and the buffer layer is discussed. We find that for a 120 nm P(VDF-TrFE)/11 nm Al_2O_3 stack in a ±20V CV loop, saturation of the polarization is almost reached. Here, we observe a very good match between the predicted and the measurement results. The application of the simulation proposed by Miller and McWorther [4] is a very useful tool to further optimize these stacks. Recently, we have shown retention of several days [15] and cycles of more than 10^5 (soon to be published). We expect even better values for optimized layers.

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